

8051-Based MCU



CGH081A

Data Sheet

8Bit Single-Chip Microcontroller
Embedded 600V 3-Phase Gate-Driver

Version: 0.0

Features

Motor Driving Engine (MDE)

- Space Vector PWM (SVPWM)
- Supports Sine-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-59° to 59° in 128 steps)
- Frequency Generator (FG)

Gate Driver

- Embedded 600V 3-phase gate-driver
- Under voltage lockout for VCC15 and VBS
- Built-in 15V/5V LDO

Embedded MCU

- MCS[®]-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
 - 2 External Interrupts (INT0N, INT1N)
 - 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
 - 8KB Flash Program Memory
 - 256 x 8-bit IRAM
 - 512 x 8-bit XRAM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- 8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU):
16*16,32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

List of Contents

Features.....2

 List of Contents3

1. Description8

2. Block Diagram8

3. Pin Assignments9

 3.1 Package Instruction LQFP7x7- 48.....9

4. Pin Definitions10

5. Absolute Maximum Ratings12

6. D.C. Characteristics12

7. A.C. Characteristics14

8. OPA Characteristics15

9. A/D Converter Characteristics.....16

10. Special Function Registers (SFR)18

 10.1 SFRs Memory Map18

 10.2 CGH081A SFRs and Reset Value19

11. Memory.....23

 11.1. Program Memory23

 11.2. Data Memory23

 11.2.1 Data Memory (IRAM)(00H~FFH).....23

 11.2.2 Data Memory (XRAM)(F000H~FOFFH).....24

12. Instruction Set25

13. MCU29

 13.1 8051 Engine.....29

 13.1.1 ACC (Accumulator)29

 13.1.2 B (B Register).....29

 13.1.3 PSW (Program Status Word Register)30

 13.1.4 SP (Stack Pointer)31

 13.1.5 DP0 (Data Pointer 0)31

 13.1.6 DP1 (Data Pointer 1)32

 13.1.7 AUX (Auxiliary Register)33

 13.1.8 RCON (Internal RAM Control Register)33

 13.2 GPIO34

 13.2.1 Port.....34

 13.2.2 PINCONG (Pin Configure Register)35

 13.2.3 PINSET (Pin I/O Setting Register)38

 13.3 Clock Structure.....40

 13.4 Timer.....41

13.4.1 PFCON (Peripheral Frequency Control Register).....	42
13.4.2 TMOD (Timer 0/1 Mode Register)	43
13.4.3 TCON (Timer 0/1 Control Register)	44
13.4.4 T2CON (Timer2 Control Register)	45
13.4.5 Timer0 Mode 0	46
13.4.6 Timer0 Mode 1	46
13.4.7 Timer0 Mode 2	46
13.4.8 Timer0 Mode 3	47
13.4.9 Timer1 Mode 0	47
13.4.10 Timer1 Mode 1	47
13.4.11 Timer1 Mode 2	48
13.4.12 Timer2 Mode 0	48
13.4.13 Timer2 Mode 1	48
13.4.14 Timer2 Mode 2	49
13.4.15 Timer2 Mode 3	49
13.5 Watchdog Timer	50
13.5.1 WDTC (Watchdog Timer Control Register)	51
13.5.2 TAKEY (Time Access Key Register).....	52
13.5.3 WDTK (Watchdog Timer Refresh Key)	52
13.6 Serial Port (UART).....	53
13.6.1 SCON (Serial Port Control Register)	55
13.6.2 SBUF (Serial Port Data Buffer).....	57
13.6.3 SREL (Serial Port Reload Register).....	57
13.7 Power Management.....	58
13.7.1 STOP MODE.....	58
13.7.2 IDLE MODE	58
13.8 Reset.....	59
13.8.1 RSTS (Reset Source Register).....	59
13.9 Interrupt Controller.....	60
13.9.1 IEN0 (Interrupt Enable Register 0)	62
13.9.2 IEN1 (Interrupt Enable Register 1)	63
13.9.3 IRCON1 (Interrupt Request Register 1)	64
13.9.4 IP (Interrupt Priority Register).....	64
14. 10-bit Analog-to-Digital Converter (ADC)	66
14.1 ADCCONT (ADC Control Register)	67
14.2 ADCSTR (ADC Start Convert and Setting Register).....	68
14.3 ADCD1 (ADC Data Register 1).....	68
14.4 ADCD2 (ADC Data Register 2).....	68
15. General PWM (GPWM).....	69

15.1 GPWMCONT (General PWM Control Register).....	70
15.2 GPWMMAX (General PWM Max Register)	70
15.3 GPWMDY (General PWM Duty Register).....	71
16. Capture.....	72
16.1 CAPCONT (Capture Control Register).....	73
16.2 CAPT (Capture Total Count)	74
16.3 CAPH (Capture High-level Count)	74
17. Addition and Subtraction Unit (ASU)	75
17.1 AS_MD_CONT (ASU and MDU Control Register).....	76
17.2 ASUD1 (ASU Data 1)	76
17.3 ASUD2 (ASU Data 2)	77
17.4 ASUR (ASU Result Register).....	78
18. Multiplication and Division Unit (MDU).....	79
18.1 AS_MD_CONT (ASU and MDU Control Register).....	79
18.2 MD_CONT (MDU Control Register).....	80
18.2.1 MDEF.....	80
18.2.2 MDOV.....	81
18.3 MD0 – MD5 (Multiplication Division Register)	81
18.4 MDU Operation Description	82
18.4.1 Loading the MDx registers	82
18.4.2 Executing calculation	83
18.4.3 Reading the result from the MDx registers.....	83
18.4.4 Shifting	84
18.4.5 Normalizing.....	84
19. Motor Driving Engine (MDE).....	85
19.1 HALL Interface Processor	86
19.2 Motor Speed Observer.....	88
19.3 Motor Angular Position Detection.....	91
19.4 Sinusoidal Data (LUT)	96
19.5 Motor Drive Signal Generator.....	96
19.6 SVPWM Engine.....	98
19.6.1 SVPWM Engine Architecture	98
19.6.2 SVPWM Current Drive.....	98
19.6.3 Motor PWM Output Setting.....	101
19.7 OCP Protection (Over Current Protection).....	108
19.7.1 OCP Block Architecture	108
19.7.2 OCP Block description and setting	108
19.8 MDE SFR List.....	112
19.8.1 MCONT1 SFR.....	112

19.8.2 MCONT2 SFR	113
19.8.3 MCONT3 SFR	113
19.8.3 HALLDBT (Hall De-bounce Time Register) SFR.....	113
19.8.4 HALLSET (Hall Setting Register 1, 2, 3) SFR	115
19.8.5 HALLST (Hall Status Register) SFR	115
19.8.6 ROTORSPEED (Rotor Speed Count Register) SFR	116
19.8.7 VRHALL (Virtual Hall Register) SFR.....	116
19.8.8 MPWM_CYC (Motor PWM Cycle Register) SFR	117
19.8.9 MPWMDY (Motor PWM Duty Register) SFR.....	118
19.8.10 MIN_DUTY (Minimum Duty Limit Register) SFR.....	119
19.8.11 MPWMDT (Motor PWM Dead-Time Register) SFR	119
19.8.12 MPWMCONT1 (MPWM Control Register 1) SFR	119
19.8.13 MPWMCONT2 (MPWM Control Register 2) SFR	120
19.8.14 MPWMINV (MPWM Inverse Selection Register) SFR	121
19.8.15 SVPWMAMP (SVPWM Amplitude Register) SFR	122
19.8.16 SVPWMAMPFT (SVPWM Amplitude Fine-Tune Register) SFR.....	122
19.8.17 SVPWMANG (SVPWM Angular Register) SFR	122
19.8.18 AS (Angle Shift Control Register) SFR.....	123
19.8.19 Over Current Protect (OCP) SFR.....	124
19.8.20 Analog Over Current Protect (AOCP) SFR.....	125
19.8.21 IMPMISC_KEY (IMPROVE Miscellaneous Function Turn On Key) SFR	125
19.8.22 IMPMISC_FUN (IMPROVE Miscellaneous Function Setting) SFR.....	126
19.8.23 ONE_HALLSET (One Hall Setting) SFR	127
19.8.24 FG_CTRL (Frequency Generator Control) SFR.....	128
19.9 SYNC	129
20. HV Gate-Driver Function Description.....	130
20.1 Low Side Power Supply (VCC15, SGND, PGND).....	130
20.2 High Side Power Supply (VBU-VSU, VBU-VSU, VBU-VSU)	131
20.3 Low Side and High Control Input Logic (HU,V,W / LU,V,W)	131
20.4 Dead-Time.....	132
20.5 Gate Driver (HOU,V,W, LOU,V,W)	132
20.6 Absolute Maximum Ratings	133
20.7 Recommended Operating Conditions.....	133
20.8 Static Electrical Characteristics	134
20.9 Dynamic Electrical Characteristics	135
21. Package Information	136
21.1 LQFP-48 7x7mm (AD48) Outline Dimensions	136
22. Marking Distinguish	137
22.1 Standard Ink (w/o code).....	137

22.2 Customization Ink (with customization code).....	137
23. Ordering Information	138
23.1 Standard Product Name.....	138
23.2 Customization Product Name	138
24. Revision History	139

1. Description

The CGH081A is a 3-phase BLDC motor controller which embedded 3-phase 600V gate-driver and supports the hall-latch interfaces. The CGH081A supports both the six-phase-drive for torque intensive application and sine-wave-drive to effectively suppress motor vibration and with the built-in, innovated speed control mechanism; an ultra-high RPM can be achieved.

The OCP protection circuitry to prevent motor damage and enhance system reliability is built-in as well. The block diagram is shown in Figure 2.1

2. Block Diagram

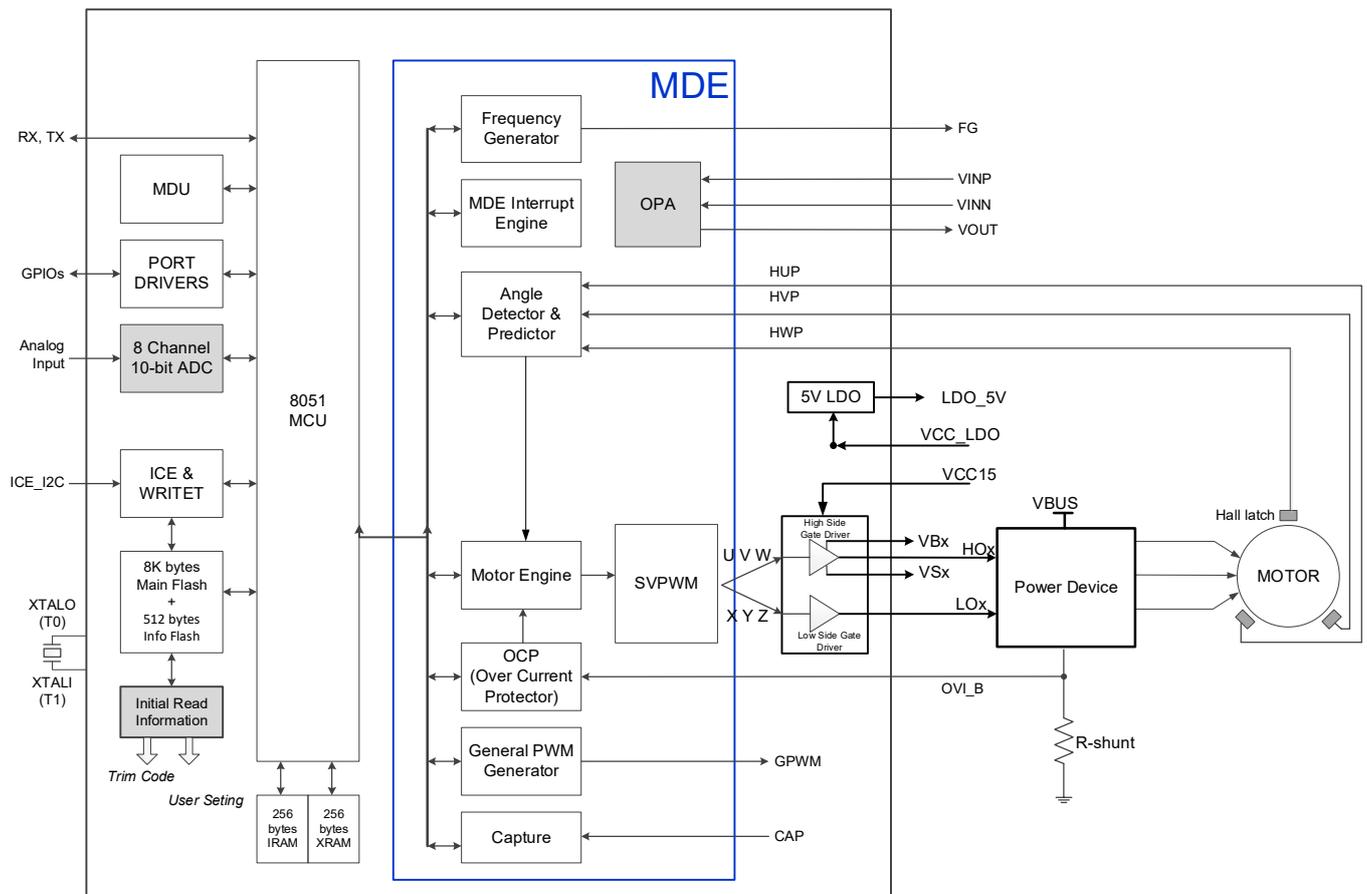
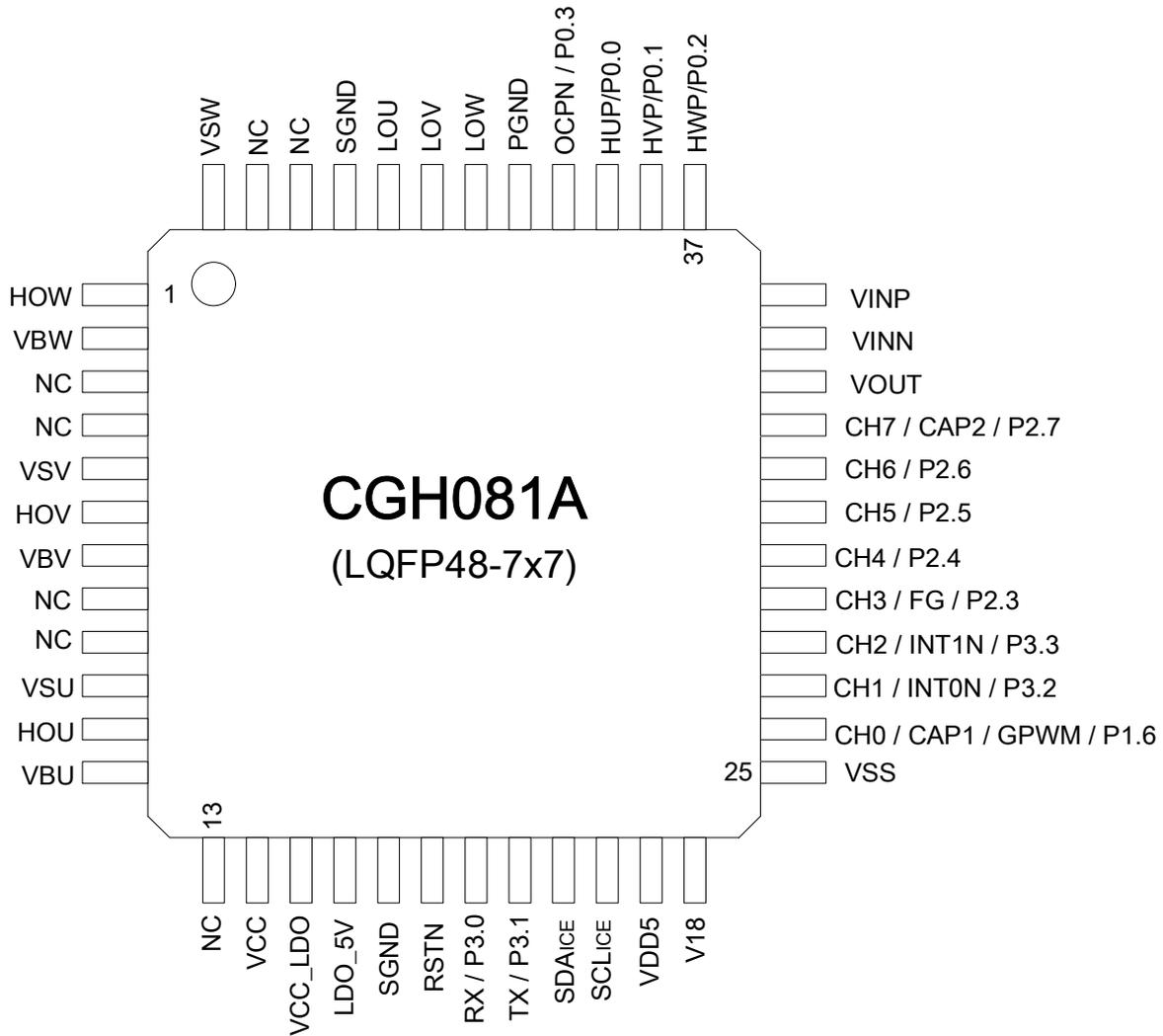


Figure 2.1 CGH081A BLDC motor controller block diagram

3. Pin Assignments

3.1 Package Instruction LQFP7x7- 48



4. Pin Definitions

Table 4.1 Pin Definitions

PIN	Name	Type	Description
48	VSU		High-side driver U-phase floating supply offset voltage
1	HOU	HV O	High-side driver U-phase gate driver output
2	VBU		High-side driver U-phase floating supply
5	VSV		High-side driver V-phase floating supply offset voltage
6	HOV	HV O	High-side driver V-phase gate driver output
7	VBV		High-side driver V-phase floating supply
10	VSW		High-side driver W-phase floating supply offset voltage
11	HOW	HV O	High-side driver W-phase gate driver output
12	VBW		High-side driver W-phase floating supply
14	VCC_LDO	Power	LDO power supply voltage
15	VCC15	Power	Logic and low-side gate drivers power supply voltage
16	LDO_5V	Power	5V LDO output
17	SGND	Ground	Logic ground
18	RSTN	I	System Reset.
33	CH7	I	Analog Input Ch7.
	CAP2	I	Capture Input 2
	P2.7	I/O	Bit 7 of Port 2.
32	CH6	I	Analog Input Ch6.
	P2.6	I/O	Bit 6 of Port 2.
31	CH5	I	Analog Input Ch5.
	P2.5	I/O	Bit 5 of Port 2.
30	CH4	I	Analog Input Ch4.
	P2.4	I/O	Bit 4 of Port 2.
29	CH3	I	Analog Input Ch3.
	FG	O	Frequency Generator Output
	P2.3	I/O	Bit 3 of Port 2.
19	RX	I	Serial Data Transmit (UART)
	P3.0	I/O	Bit 0 of Port 3.
20	TX	O	Serial Data Receive (UART)
	P3.1	I/O	Bit 1 of Port 3.
21	SDA _{ICE}		For ICE (In Circuit Emulator).
22	SCL _{ICE}		For ICE (In Circuit Emulator).
23	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be

			connected between this pin and VSS.
24	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
25	VSS	Ground	Power Ground.
26	CH0	I	Analog Input Ch0.
	CAP1	I	Capture Input 1
	GPWM	O	General PWM output.
	P1.6	I/O	Bit 6 of Port 1.
27	CH1	I	Analog Input Ch1.
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
	P3.2	I/O	Bit 2 of Port 3.
28	CH2	I	Analog Input Ch2.
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.
	P3.3	I/O	Bit 3 of Port 3.
37	HWP	I	Hall Latch input positive input. (HALL W)
	P0.2	I/O	Bit 2 of Port 0.
38	HVP	I	Hall Latch input positive input. (HALL V)
	P0.1	I/O	Bit 1 of Port 0.
34	VOUT	O	OPA output
35	VINN	I	OPA input (-)
36	VINP	I	OPA input (+)
39	HUP	I	Hall Latch input positive input.(HALL U)
	P0.0	I/O	Bit 0 of Port 0.
40	OCPN	I	Over current protection. Active-low.
	P0.3	I/O	Bit 3 of Port 0.
41	PGND	Ground	Low-side gate drivers ground
42	LOU	O	Low-side gate driver U-phase output
43	LOV	O	Low-side gate driver V-phase output
44	LOW	O	Low-side gate driver W-phase output
45	SGND	Ground	Logic ground