CGH081A

Data Sheet

8Bit Single-Chip Microcontroller

Embedded 600V 3-Phase Gate-Driver

Version: 0.0

2024/3 version 0.0

Features

Motor Driving Engine (MDE)

- Space Vector PWM (SVPWM)
- Supports Sine-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-59° to 59° in 128 steps)
- Frequency Generator (FG)

Gate Driver

- Embedded 600V 3-phase gate-driver
- Under voltage lockout for VCC15 and VBS
- Built-in 15V/5V LDO

Embedded MCU

- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
  - 2 External Interrupts (INT0N, INT1N)
  - 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 8KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
  8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bitnormalization

List of Contents

1. Description

The CGH081A is a 3-phase BLDC motor controller which embedded 3-phase 600V gate-driver and supports the hall-latch interfaces. The CGH081A supports both the six-phase-drive for torque intensive application and sine-wave-drive to effectively suppress motor vibration and with the built-in, innovated speed control mechanism; an ultra-high RPM can be achieved.

The OCP protection circuitry to prevent motor damage and enhance system reliability is built-in as well. The block diagram is shown in Figure 2.1

2. Block Diagram

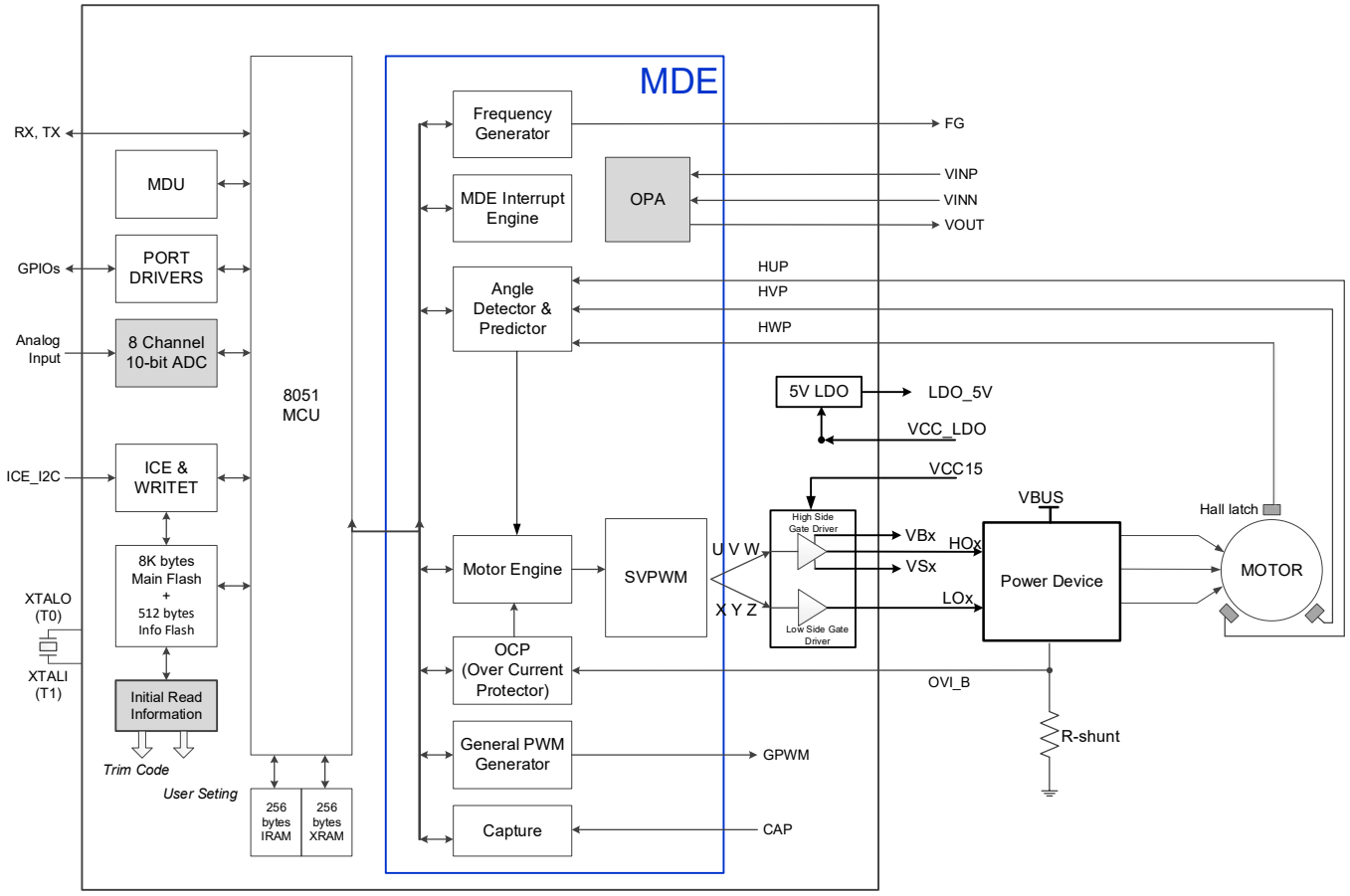
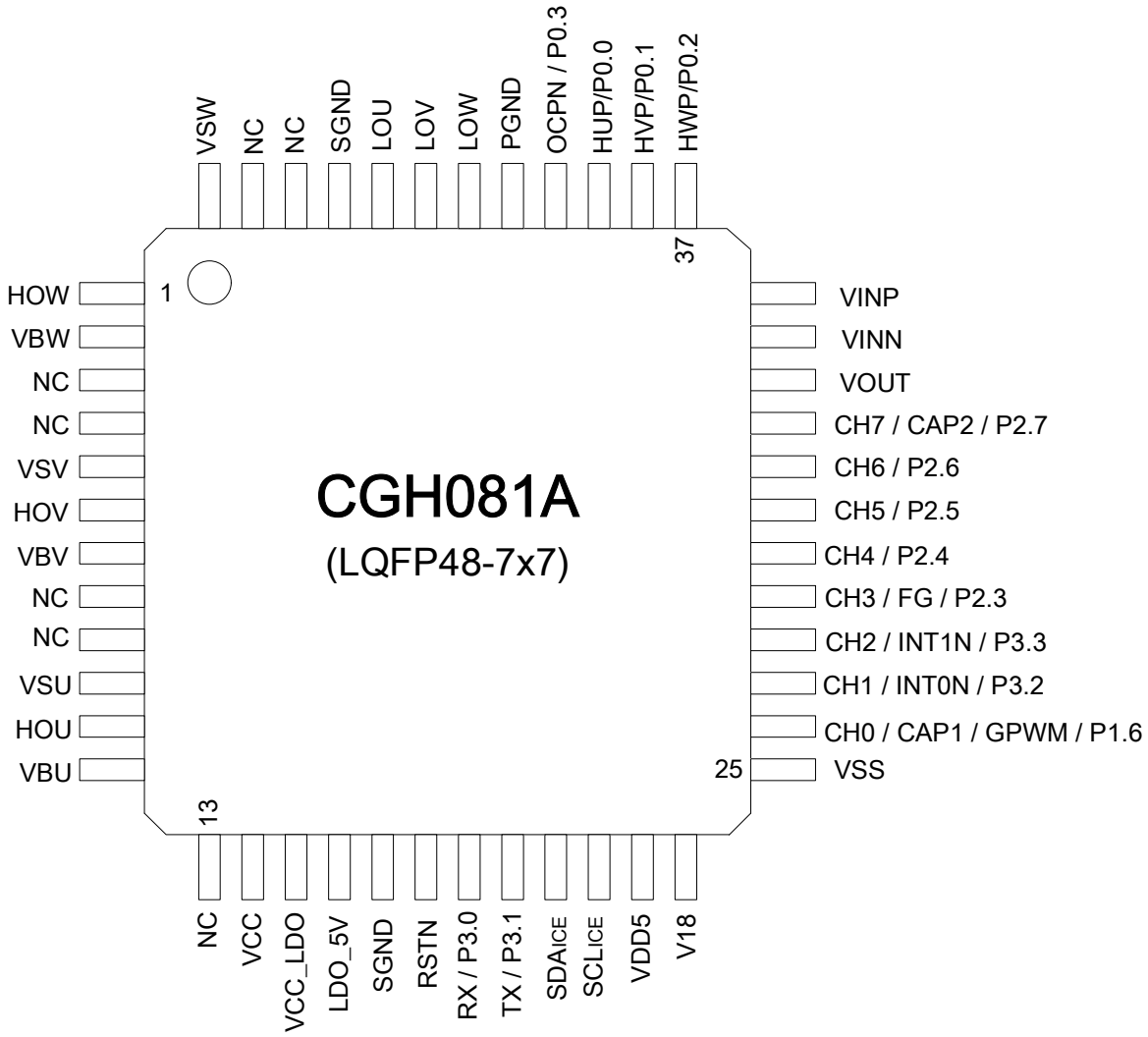


Figure 2.1 CGH081A BLDC motor controller block diagram

3. Pin Assignments

3.1 Package Instruction LQFP7x7- 48



4. Pin Definitions

Table 4.1 Pin Definitions

PIN	Name	Type	Description
48	VSU		High-side driver U-phase floating supply offset voltage
1	HOU	HV O	High-side driver U-phase gate driver output
2	VBU		High-side driver U-phase floating supply
5	VSV		High-side driver V-phase floating supply offset voltage
6	HOV	HV O	High-side driver V-phase gate driver output
7	VBV		High-side driver V-phase floating supply
10	VSW		High-side driver W-phase floating supply offset voltage
11	HOW	HV O	High-side driver W-phase gate driver output
12	VBW		High-side driver W-phase floating supply
14	VCC_LDO	Power	LDO power supply voltage
15	VCC15	Power	Logic and low-side gate drivers power supply voltage
16	LDO_5V	Power	5V LDO output
17	SGND	Ground	Logic ground
18	RSTN	I	System Reset.
33	CH7	I	Analog Input Ch7.
	CAP2	I	Capture Input 2
	P2.7	I/O	Bit 7 of Port 2.
32	CH6	I	Analog Input Ch6.
	P2.6	I/O	Bit 6 of Port 2.
31	CH5	I	Analog Input Ch5.
	P2.5	I/O	Bit 5 of Port 2.
30	CH4	I	Analog Input Ch4.
	P2.4	I/O	Bit 4 of Port 2.
29	CH3	I	Analog Input Ch3.
	FG	O	Frequency Generator Output
	P2.3	I/O	Bit 3 of Port 2.
19	RX	I	Serial Data Transmit (UART)
	P3.0	I/O	Bit 0 of Port 3.
20	TX	O	Serial Data Receive (UART)
	P3.1	I/O	Bit 1 of Port 3.
21	SDA_{ICE}		For ICE (In Circuit Emulator).
22	SCL_{ICE}		For ICE (In Circuit Emulator).
23	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be

			connected between this pin and VSS.
24	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
25	VSS	Ground	Power Ground.
26	CH0	I	Analog Input Ch0.
	CAP1	I	Capture Input 1
	GPWM	O	General PWM output.
	P1.6	I/O	Bit 6 of Port 1.
27	CH1	I	Analog Input Ch1.
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
	P3.2	I/O	Bit 2 of Port 3.
28	CH2	I	Analog Input Ch2.
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.
	P3.3	I/O	Bit 3 of Port 3.
37	HWP	I	Hall Latch input positive input. (HALL W)
	P0.2	I/O	Bit 2 of Port 0.
38	HVP	I	Hall Latch input positive input. (HALL V)
	P0.1	I/O	Bit 1 of Port 0.
34	VOUT	O	OPA output
35	VINN	I	OPA input (-)
36	VINP	I	OPA input (+)
39	HUP	I	Hall Latch input positive input.(HALL U)
	P0.0	I/O	Bit 0 of Port 0.
40	OCPN	I	Over current protection. Active-low.
	P0.3	I/O	Bit 3 of Port 0.
41	PGND	Ground	Low-side gate drivers ground
42	LOU	O	Low-side gate driver U-phase output
43	LOV	O	Low-side gate driver V-phase output
44	LOW	O	Low-side gate driver W-phase output
45	SGND	Ground	Logic ground