# CGH021A

# Data Sheet

*8Bit Single-Chip Microcontroller*

*Embedded 40V 3-Phase Gate-Driver*

**Version: 0.0**

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# Features

**Motor Driving Engine (MDE)**

- Space Vector PWM (SVPWM)
- Supports Sine-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-59° to 59° in 128 steps)
- Frequency Generator (FG)

**Gate Driver**

- Integrated 40V 3-phase P/N MOSFET Pre-driver
- Shoot-through protection
- Built-in 5V LDO

**Embedded MCU**

- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
  - 2 External Interrupts (INT0N, INT1N)
  - 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 8KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
  8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bitnormalization

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# 1. Description

The CGH021A is a 3-phase BLDC motor controller which embedded 3-phase 40V P/N gate-driver and supports the hall-latch interfaces. The CGH021A supports both the six-phase-drive for torque intensive application and sine-wave-drive to effectively suppress motor vibration and with the built-in, innovated speed control mechanism; an ultra-high RPM can be achieved.

The OCP protection circuitry to prevent motor damage and enhance system reliability is built-in as well. The block diagram is shown in Figure 2.1

# 2. Block Diagram

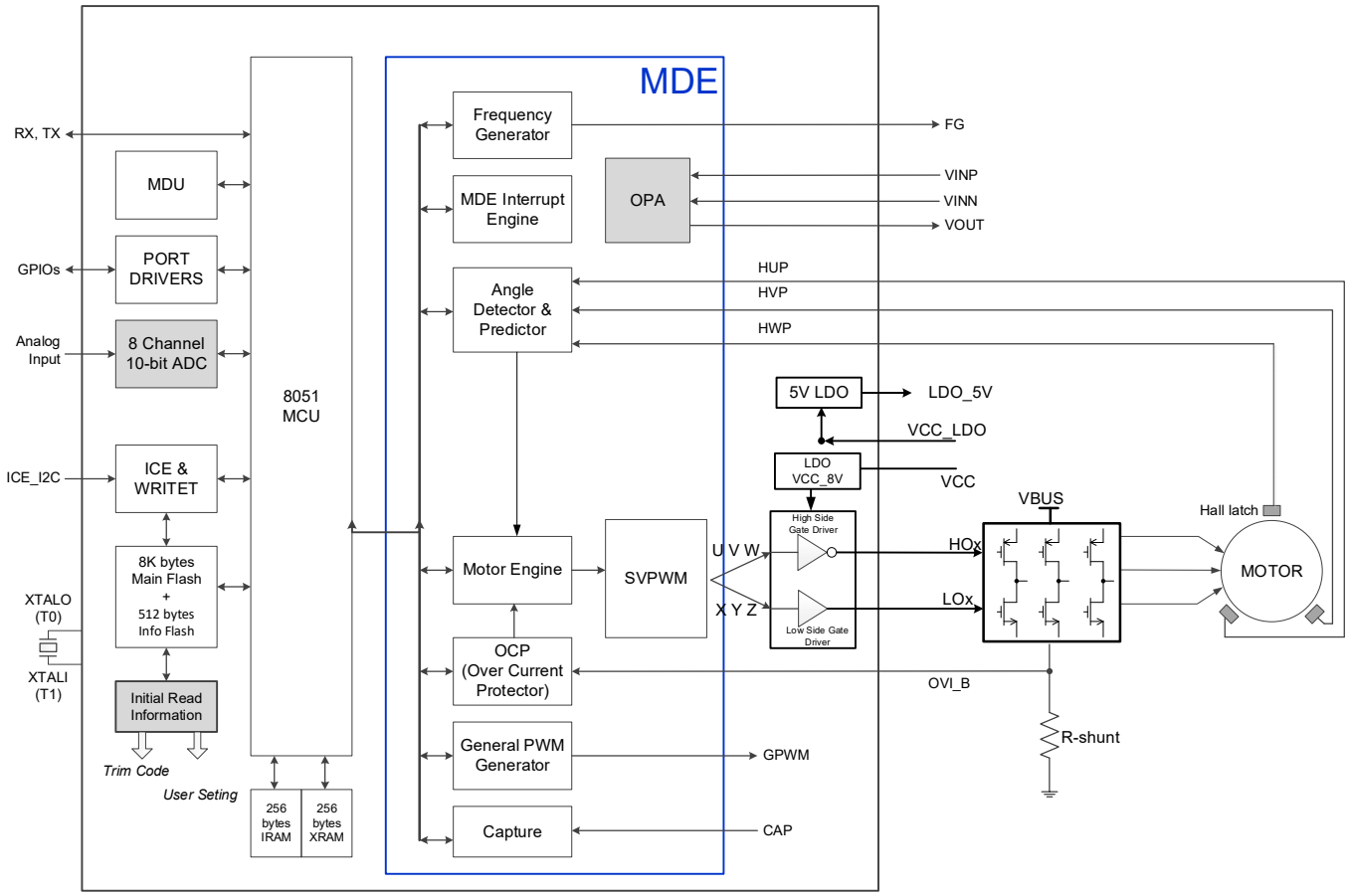
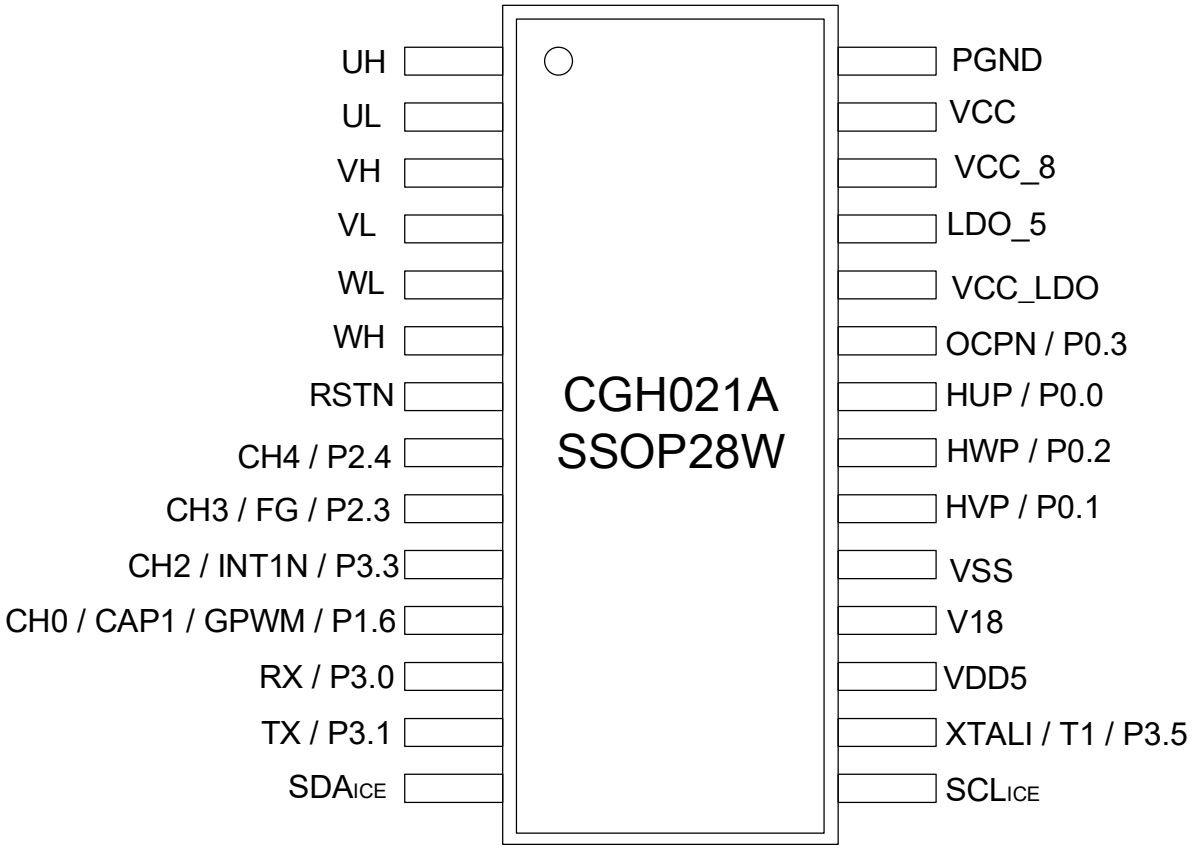


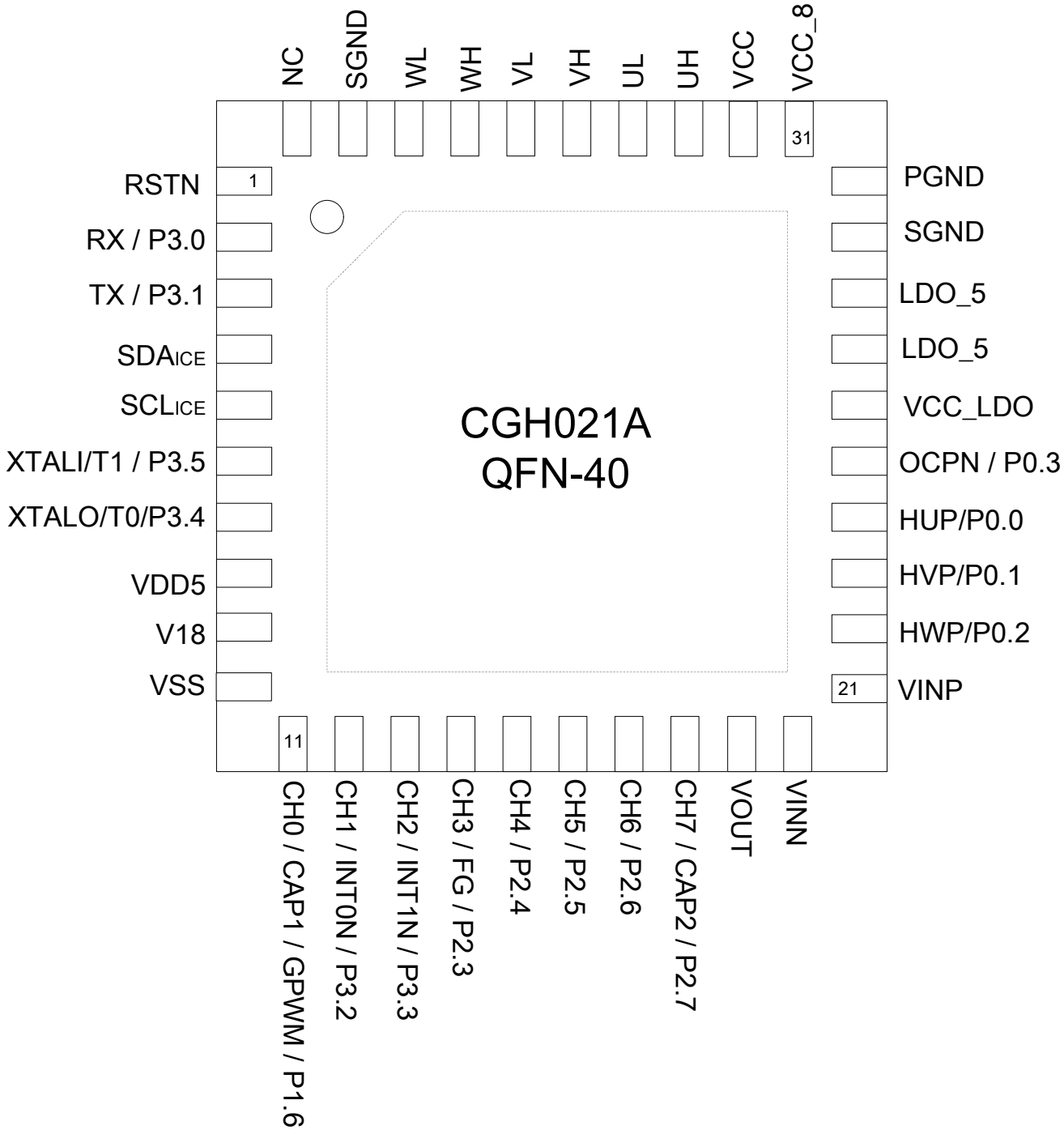

Figure 2.1 CGH021A BLDC motor controller block diagram

# 3. Pin Assignments

## 3.1 Package Instruction SSOP28W (209mil)



## 3.2 Package Instruction QFN40-5X5mm



# 4. Pin Definitions

Table 4.1 Pin Definitions

| SSOP28W PIN N.O. | QFN40 PIN N.O. | Name | Type | Description |
|---|---|---|---|---|
| 27 | 32 | VCC | Power | Supply voltage input. |
| 1 | 33 | UH | O | High side phase-U PMOS driver. |
| 2 | 34 | UL | O | Low side phase-U NMOS driver. |
| 3 | 35 | VH | O | High side phase-V PMOS driver. |
| 4 | 36 | VL | O | Low side phase-V NMOS driver. |
| 6 | 37 | WH | O | High side phase-W PMOS driver. |
| 5 | 38 | WL | O | Low side phase-W NMOS driver. |
| 24 | 26 | VCC_LDO | Power | LDO 5V power supply. |
| 25 | 27 / 28 | LDO_5 | Power | 5V output of LDO. |
| 28 | 30 | PGND | Ground | Power ground. |
| 26 | 31 | VCC_8 | O | LDO VCC_8 output |
| -- | 29 / 39 | SGND | Ground | Logic ground |
| 7 | 1 | RSTN | I | System Reset. |
| -- | 18 | CH7 | I | Analog Input Ch7. |
| | | CAP2 | I | Capture Input 2 |
| | | P2.7 | I/O | Bit 7 of Port 2. |
| -- | 17 | CH6 | I | Analog Input Ch6. |
| | | P2.6 | I/O | Bit 6 of Port 2. |
| -- | 16 | CH5 | I | Analog Input Ch5. |
| | | P2.5 | I/O | Bit 5 of Port 2. |
| 8 | 15 | CH4 | I | Analog Input Ch4. |
| | | P2.4 | I/O | Bit 4 of Port 2. |
| 9 | 14 | CH3 | I | Analog Input Ch3. |
| | | FG | O | Frequency Generator Output |
| | | P2.3 | I/O | Bit 3 of Port 2. |
| 12 | 2 | RX | I | Serial Data Transmit (UART) |
| | | P3.0 | I/O | Bit 0 of Port 3. |
| 13 | 3 | TX | O | Serial Data Receive (UART) |
| | | P3.1 | I/O | Bit 1 of Port 3. |
| 14 | 4 | $SDA_{ICE}$ | | For ICE (In Circuit Emulator). |
| 15 | 5 | $SCL_{ICE}$ | | For ICE (In Circuit Emulator). |
| 17 | 8 | VDD5 | Power | 5.0V Voltage Input. A 0.1uF and 10uF (minimum) |

| | | | | |
|---|---|---|---|---|
| | | | | capacitor should be connected between this pin and VSS. |
| 18 | 9 | V18 | O | 1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS. |
| 19 | 10 | VSS | Ground | Power Ground. |
| 11 | 11 | CH0 | I | Analog Input Ch0. |
| | | CAP1 | I | Capture Input 1 |
| | | GPWM | O | General PWM output. |
| | | P1.6 | I/O | Bit 6 of Port 1. |
| -- | 12 | CH1 | I | Analog Input Ch1. |
| | | INT0N | I | External Interrupt 0. Low level trigger or falling edge trigger. |
| | | P3.2 | I/O | Bit 2 of Port 3. |
| 10 | 13 | CH2 | I | Analog Input Ch2. |
| | | INT1N | I | External Interrupt 1. Low level trigger or falling edge trigger. |
| | | P3.3 | I/O | Bit 3 of Port 3. |
| 21 | 22 | HWP | I | Hall Latch input positive input. (HALL W) |
| | | P0.2 | I/O | Bit 2 of Port 0. |
| 20 | 23 | HVP | I | Hall Latch input positive input. (HALL V) |
| | | P0.1 | I/O | Bit 1 of Port 0. |
| -- | 19 | VOUT | O | OPA output |
| -- | 20 | VINN | I | OPA input (-) |
| -- | 21 | VINP | I | OPA input (+) |
| 22 | 24 | HUP | I | Hall Latch input positive input.(HALL U) |
| | | P0.0 | I/O | Bit 0 of Port 0. |
| 23 | 25 | OCPN | I | Over current protection. Active-low. |
| | | P0.3 | I/O | Bit 3 of Port 0. |
| 16 | 6 | XTALI | I | Crystal input pin. Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS. |
| | | T1 | I | TIMER1 External Input. |
| | | P3.5 | I/O | Bit 5 of Port 3. |
| -- | 7 | XTALO | O | Crystal output pin. Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS. |
| | | T0 | I | TIMER0 External Input. |
| | | P3.4 | I/O | Bit 4 of Port 3. |