

8051-Based MCU



CGH001A

8Bit Single-Chip Microcontroller

Data Sheet

Version: 0.0

Features

Motor Driving Engine (MDE)

- Space Vector PWM (SVPWM)
- Supports Sine-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-59° to 59° in 128 steps)
- Frequency Generator (FG)

Embedded MCU

- MCS[®]-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 14 Interrupt Sources
- 1 External Interrupts (INT1N)
- Memory Size:
 - 8KB Flash Program Memory
 - 256 x 8-bit IRAM
 - 256 x 8-bit XRAM
- Up to 22 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- 1-Channel 16-bit Capture
- 8-Channel 10-bit Analog-to-Digital Converter (ADC)
- General Operational Amplifier
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

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1. Description

The CGH001A is a 3-phase BLDC motor controller which supports the hall-latch interfaces. The CGH001A supports both the six-phase-drive for torque intensive application and sine-wave-drive to effectively suppress motor vibration and with the built-in, innovated speed control mechanism; an ultra-high RPM can be achieved.

The OCP protection circuitry to prevent motor damage and enhance system reliability is built-in as well. The block diagram is shown in Figure 2.1

2. Block Diagram

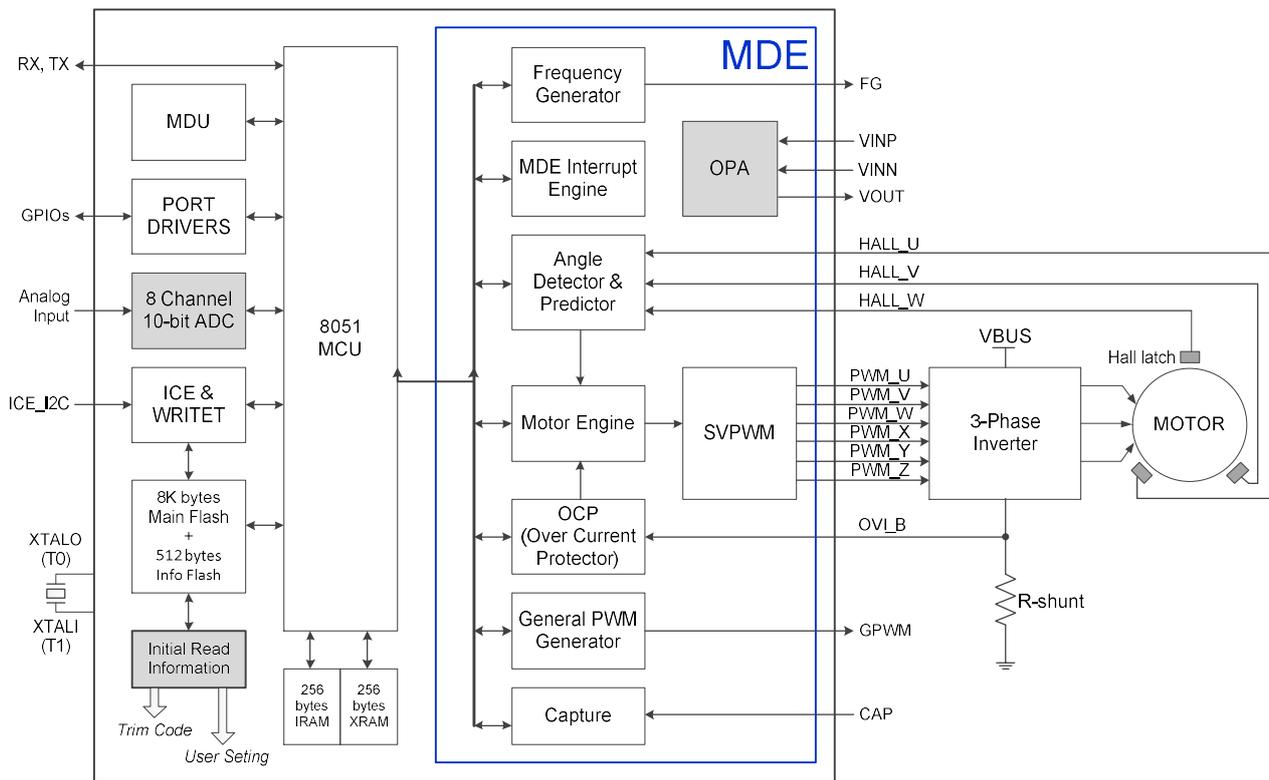


Figure 2.1 CGH001A BLDC motor controller block diagram

3. Pin Assignments

3.1 SSOP-28(AL28)

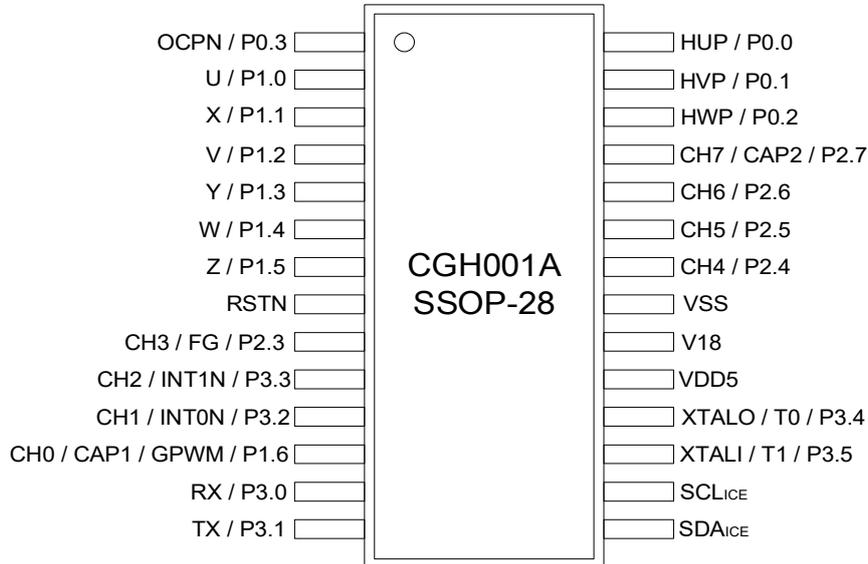


Figure 3.1 SSOP-28(AD4)

3.2 QFN32-4x4mm (AZ32)

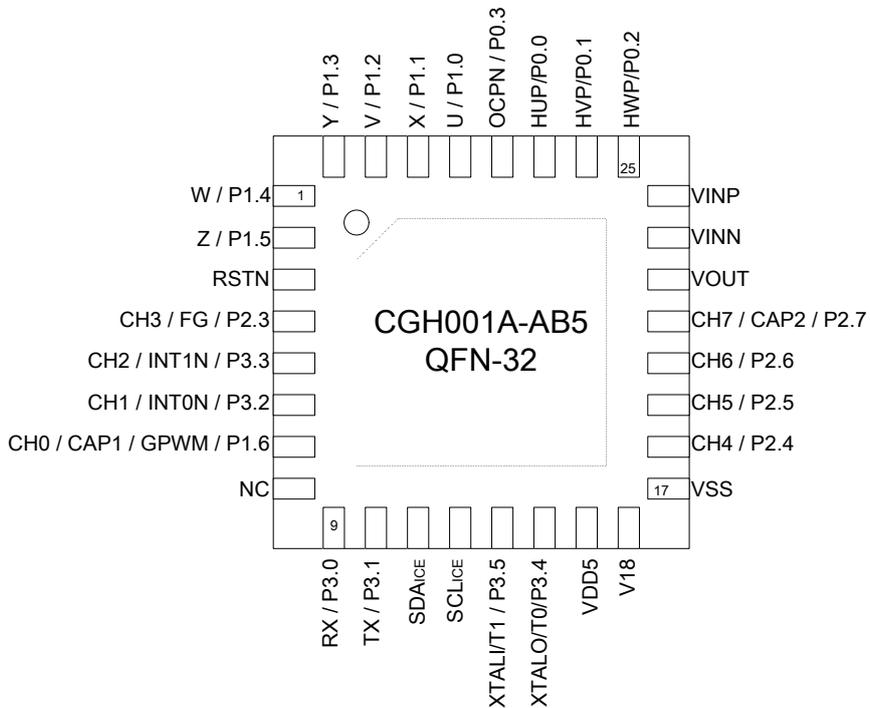


Figure 3.2 QFN32 4X4 (AB5)

4. Pin Definitions

Table 4.1 Pin Definitions

SSOP28	QFN32			
PIN #		Name	Type	Description
8	3	RSTN	I	System Reset.
25	21	CH7	I	Analog Input Ch7.
		CAP2	I	Capture Input 2
		P2.7	I/O	Bit 7 of Port 2.
24	20	CH6	I	Analog Input Ch6.
		P2.6	I/O	Bit 6 of Port 2.
23	19	CH5	I	Analog Input Ch5.
		P2.5	I/O	Bit 5 of Port 2.
22	18	CH4	I	Analog Input Ch4.
		P2.4	I/O	Bit 4 of Port 2.
9	4	CH3	I	Analog Input Ch3.
		FG	O	Frequency Generator Output
		P2.3	I/O	Bit 3 of Port 2.
13	9	RX	I	Serial Data Transmit (UART)
		P3.0	I/O	Bit 0 of Port 3.
14	10	TX	O	Serial Data Receive (UART)
		P3.1	I/O	Bit 1 of Port 3.
15	11	SDA _{ICE}		For ICE (In Circuit Emulator).
16	12	SCL _{ICE}		For ICE (In Circuit Emulator).
17	13	XTALI	I	Crystal input pin. Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS.
		T1	I	TIMER1 External Input.
		P3.5	I/O	Bit 5 of Port 3.
18	14	XTALO	O	Crystal output pin. Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS.
		T0	I	TIMER0 External Input.
		P3.4	I/O	Bit 4 of Port 3.
---	8	NC		No connect.
19	15	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.
20	16	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.

21	17	VSS	Ground	Power Ground.
12	7	CH0	I	Analog Input Ch0.
		CAP1	I	Capture Input 1
		GPWM	O	General PWM output.
		P1.6	I/O	Bit 6 of Port 1.
11	6	CH1	I	Analog Input Ch1.
		INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
		P3.2	I/O	Bit 2 of Port 3.
10	5	CH2	I	Analog Input Ch2.
		INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.
		P3.3	I/O	Bit 3 of Port 3.
26	25	HWP	I	Hall Latch input (HALL W)
		P0.2	I/O	Bit 2 of Port 0.
27	26	HVP	I	Hall Latch input (HALL V)
		P0.1	I/O	Bit 1 of Port 0.
---	22	VOUT	O	OPA output
---	23	VINN	I	OPA input (-)
---	24	VINP	I	OPA input (+)
28	27	HUP	I	Hall Latch input (HALL U)
		P0.0	I/O	Bit 0 of Port 0.
1	28	OCPN	I	Over current protection. Active-low.
		P0.3	I/O	Bit 3 of Port 0.
2	29	U	O	PWM output. High-side PWM of phase U.
		P1.0	I/O	Bit 0 of Port 1.
3	30	X	O	PWM output. Low-side PWM of phase U.
		P1.1	I/O	Bit 1 of Port 1.
4	31	V	O	PWM output. High-side PWM of phase V.
		P1.2	I/O	Bit 2 of Port 1.
5	32	Y	O	PWM output. Low-side PWM of phase V.
		P1.3	I/O	Bit 3 of Port 1.
6	1	W	O	PWM output. High-side PWM of phase W.
		P1.4	I/O	Bit 4 of Port 1.
7	2	Z	O	PWM output. Low-side PWM of phase W.
		P1.5	I/O	Bit 5 of Port 1.