

**8051-Based MCU**



# **CGF062A**

## **Data Sheet**

*8Bit Single-Chip Microcontroller  
Embedded 200V 3-Phase Gate-Driver*

**Version: V0.0**

## Features

### Motor Driving Engine (MDE)

- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC) Sine-Wave Solutions
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Position Detection (IPD)
- Programmable Dead-Time
- Independent PI Controller
- Independent General Low Pass Filter
- Frequency Generator

### Gate Driver

- Embedded 200V 3-phase gate-driver
- Under voltage lockout for VCC15 and VBS
- Built-in 15V/5V LDO

### Embedded MCU

- MCS<sup>®</sup>-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
- 2 External Interrupts (INT0N, INT1N)
- 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 16KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- 256 Byte EEPROM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- 8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- IIC Interface (Master/Slave Mode)
- One Wire RF/IR Receiver Output Signal Decode
- CRC16-CCITT Function
- Independent General PWM
- External Capture
- Internal Capture
- Fast Multiplication-Division Unit (MDU):  
16\*16,32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

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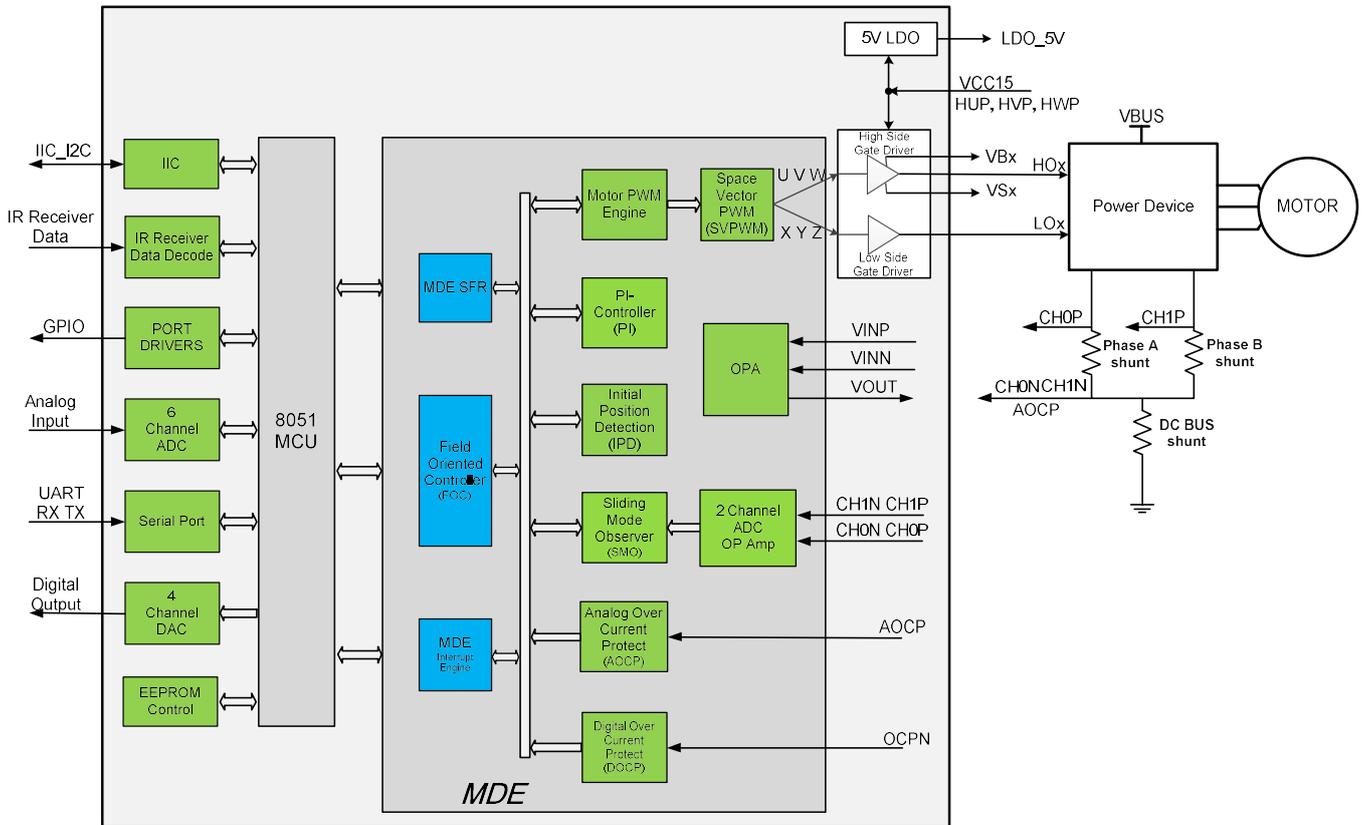
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## 1. General Description

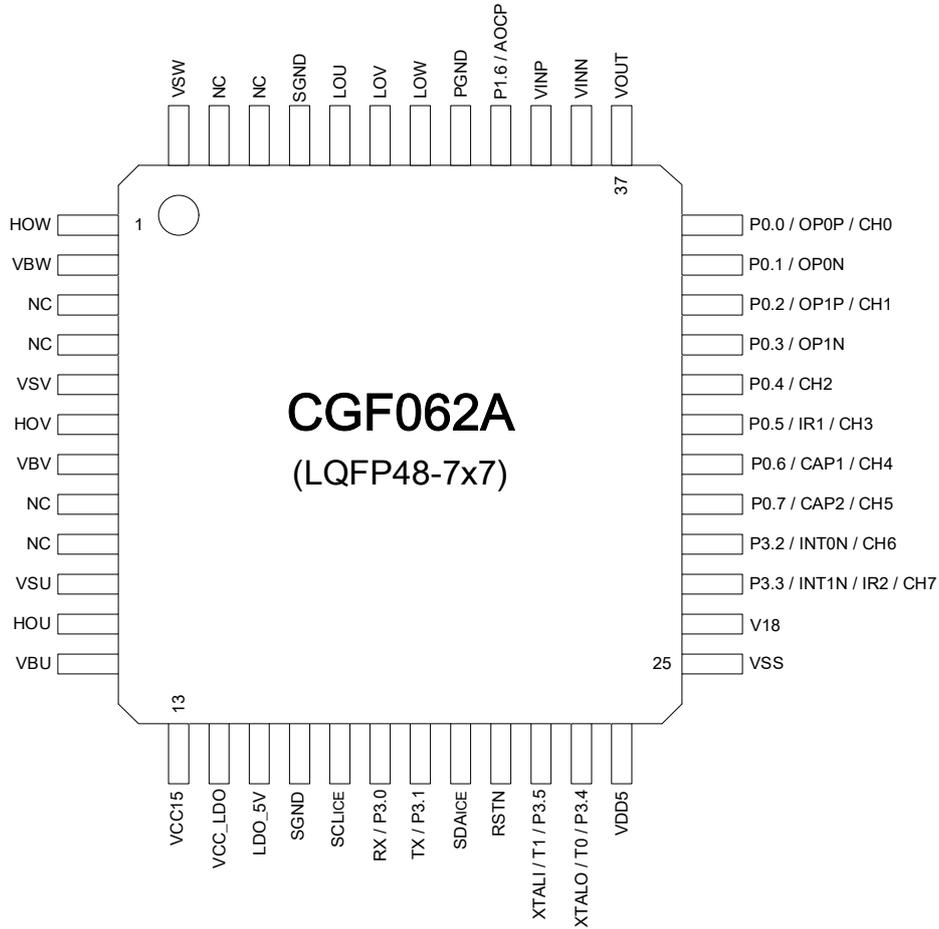
The CGF062A is a highly integrated motor drive controller. The CGF062A is composed of FOC sensor-less MCU and 200V 3-phase Gate-Driver that suit for under DC 400V and medium motor system, for example household fan, water pump, industry fan...etc.

## 2. Block Diagram



### 3. Pin Configurations

#### 3.1. Package Instruction LQFP7x7- 48



### 3.2. Pin Description

Table 3.1. Pin Description

Pin # CGF062A LQFP-48	Name	Type	Description
10	VSU		High-side driver U-phase floating supply offset voltage
11	HOU	HV O	High-side driver U-phase gate driver output
12	VBU		High-side driver U-phase floating supply
5	VSV		High-side driver V-phase floating supply offset voltage
6	HOV	HV O	High-side driver V-phase gate driver output
7	VBV		High-side driver V-phase floating supply
48	VSW		High-side driver W-phase floating supply offset voltage
1	HOW	HV O	High-side driver W-phase gate driver output
2	VBW		High-side driver W-phase floating supply
13	VCC15	Power	Logic and low-side gate drivers power supply voltage
14	VCC_LDO	Power	LDO power supply voltage
15	LDO_5V	Power	5V LDO output
16	SGND	Ground	Logic ground
18	P3.0	I/O	Bit 0 of Port 3.
	RX	I	Serial Data Transmit (UART)
19	P3.1	I/O	Bit 1 of Port 3.
	TX	O	Serial Data Receive (UART)
28	P3.2	I/O	Bit 2 of Port 3.
	CH6	I	Analog Input Ch6.
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
27	P3.3	I/O	Bit 3 of Port 3.
	CH7	I	Analog Input Ch7.
	IR2	I	IR receiver signal input 2
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.

23	P3.4	I/O	Bit 4 of Port 3.
	XTALO	O	Crystal output pin. Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS.
	T0	I	TIMER0 External Input.
22	P3.5	I/O	Bit 5 of Port 3.
	XTALI	I	Crystal input pin. Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS.
	T1	I	TIMER1 External Input.
24	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.
25	VSS	Ground	Power Ground.
26	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
29	P0.7	I/O	Bit 7 of Port 0.
	CH5	I	Analog Input Ch5.
	CAP2	I	Capture Input 2.
30	P0.6	I/O	Bit 6 of Port 0.
	CH4	I	Analog Input Ch4.
	CAP1	I	Capture Input 1
31	P0.5	I/O	Bit 5 of Port 0.
	CH3	I	Analog Input Ch3.
	IR1	I	IR receiver signal input 1
32	P0.4	I/O	Bit 2 of Port 0.
	CH2	I	Analog Input Ch2.
33	P0.3	I/O	Bit 2 of Port 0.
	OP1N	I	OP 1-Amp N-Input.
34	P0.2	I/O	Bit 3 of Port 0.
	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	O	OP 1-Amp P- Input
35	P0.1	I/O	Bit 0 of Port 0.
	OP0N	I	OP 0-Amp N- Input.
36	P0.0	I/O	Bit 1 of Port 0.
	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP 0-Amp P-Input.

37	OP_VOUT	O	OPA output
38	OP_VINN	I	OPA N-Input
39	OP_VINP	I	OPA P-Input
40	P1.6	I/O	Bit 6 of Port 1.
	AOCP	I	Analog OCP Control.
21	RSTN	I	System Reset.
20	SDA <sub>ICE</sub>		For ICE.
17	SCL <sub>ICE</sub>		For ICE.
41	PGND	Ground	Low-side gate drivers ground
45	SGND	Ground	Logic ground
44	LOU	O	Low-side gate driver U-phase output
43	LOV	O	Low-side gate driver V-phase output
42	LOW	O	Low-side gate driver W-phase output