CGF022A
Data Sheet

8Bit Single-Chip Microcontroller
Embedded 40V 3-Phase Gate-Driver

Version: V0.0

Features

Motor Driving Engine (MDE)

- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC) Sine-Wave Solutions
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Position Detection (IPD)
- Programmable Dead-Time
- Independent PI Controller
- Independent General Low Pass Filter
- Frequency Generator

Gate Driver

- Integrated 40V 3-phase P/N MOSFET Pre-driver
- Shoot-through protection
- Built-in 5V LDO
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Embedded MCU

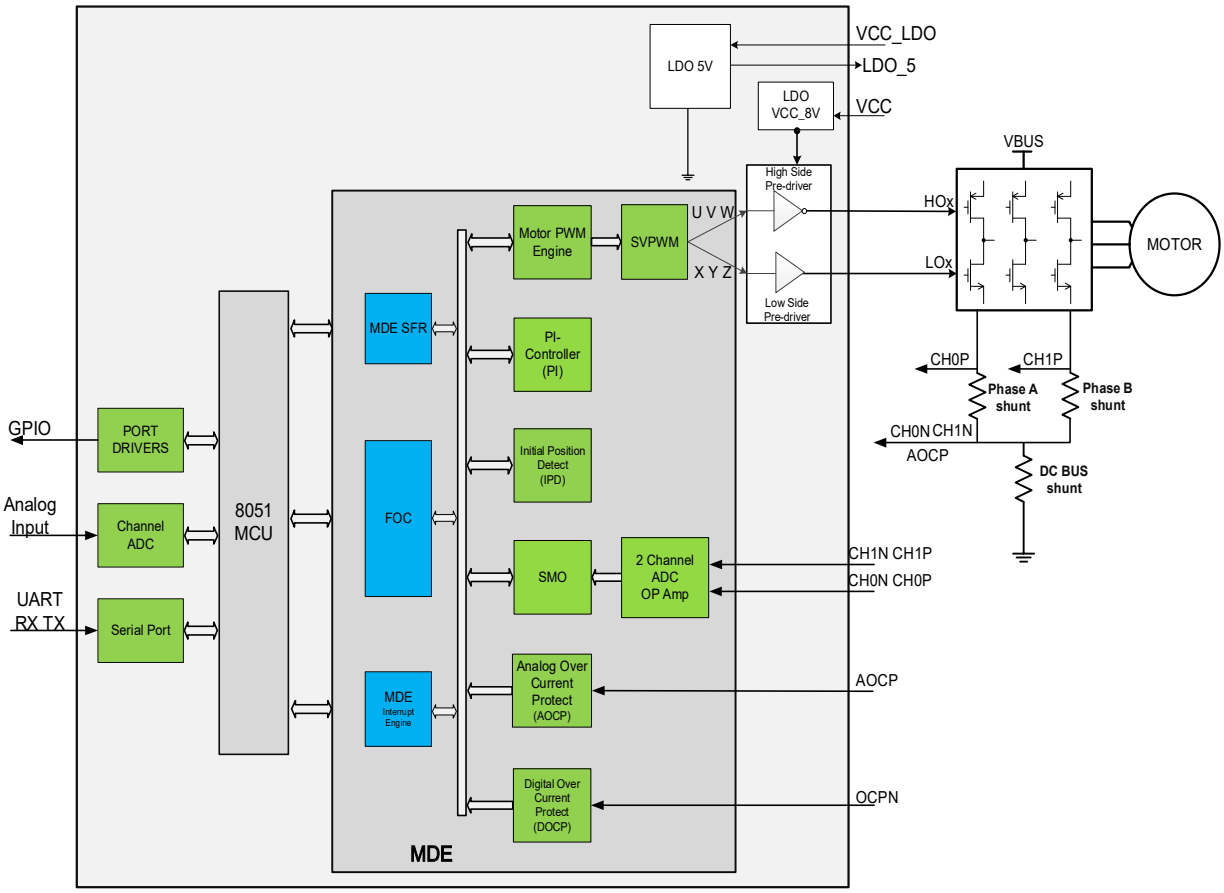
- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
- 2 External Interrupts (INT0N, INT1N)
- 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 16KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- 256 Byte EEPROM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
  8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- IIC Interface (Master/Slave Mode)
- One Wire RF/IR Receiver Output Signal Decode
- CRC16-CCITT Function
- Independent General PWM
- External Capture
- Internal Capture
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bitnormalization

List of Contents

1. General Description

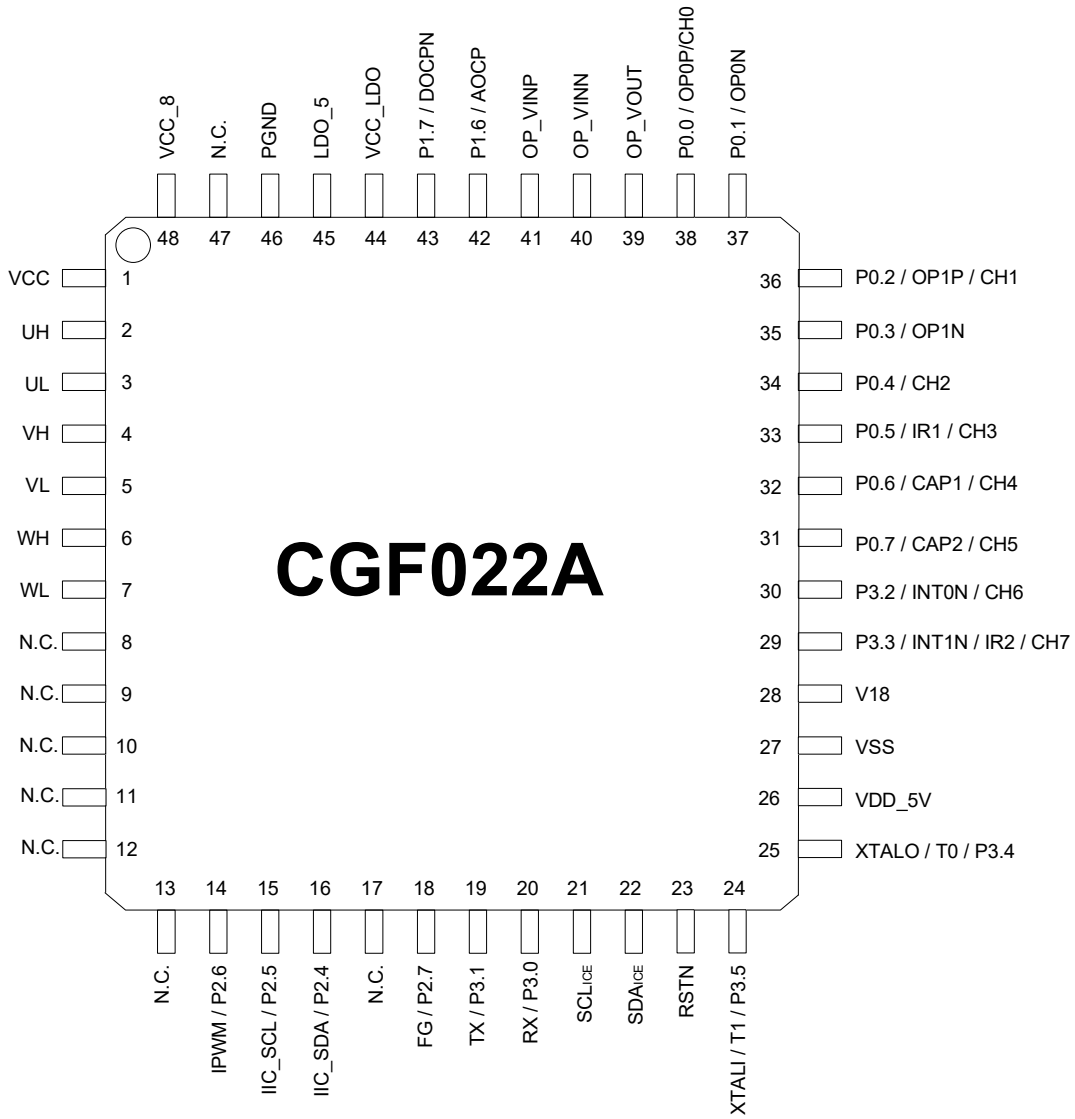
The CGF022A is a highly integrated motor drive controller. The CGF022A is composed of FOC sensor-less MCU and 40V 3-phase P/N Gate-Driver that suit for under DC 40V and medium motor system, for example household fan、water pump、industry fan…etc.

2. Block Diagram



3. Pin Configurations

3.1. Package Instruction LQFP7x7- 48



3.2. Pin Description

Table 3.1. Pin Description

Pin #	Name	Type	Description
1	VCC	Power	Supply voltage input.
2	UH	O	High side phase-U PMOS driver.
3	UL	O	Low side phase-U NMOS driver.
4	VH	O	High side phase-V PMOS driver.
5	VL	O	Low side phase-V NMOS driver.
6	WH	O	High side phase-W PMOS driver.
7	WL	O	Low side phase-W NMOS driver.
8	NC		
9	NC		
10	NC		
11	NC		
12	NC		
13	NC		
14	P2.6	I/O	Bit6 of Port 2.
	IPWM	O	Independent User PWM Output
15	P2.5	I/O	Bit5 of Port 2.
	IIC_SCL	O	IIC clock
16	P2.4	I/O	Bit4 of Port 2.
	IIC_SDA	O	IIC data
17	NC		
18	P2.7	I/O	Bit7 of Port 2.
	FG	O	Function Generate Output
19	P3.1	I/O	Bit1 of Port 3.
	TX	O	Serial Data Receive (UART)
20	P3.0	I/O	Bit0 of Port 3.
	RX	I	Serial Data Transmit (UART)
21	SCL_{ICE}		For ICE.
22	SDA_{ICE}		For ICE.
23	RSTN	I	System Reset.
24	P3.5	I/O	Bit 5 of Port 3
	XTALI	I	Crystal input pin. **Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS**
	T1	I	TIMER1 External Input
25	P3.4	I/O	Bit 4 of Port 3
	XTALO	O	Crystal output pin. **Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS**
	T0	I	TIMER0 External Input
26	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.
27	VSS	Ground	Power Ground.
28	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
29	P3.3	I/O	Bit 3 of Port 3
	CH7	I	Analog Input Ch7

	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger
	IR2	I	IR receiver signal input 2
30	P3.2	I/O	Bit2 of Port 3
	CH6	I	Analog Input Ch6
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger
31	P0.7	I/O	Bit7 of Port 0
	CH5	I	Analog Input Ch5
	CAP2	I	Capture Input 2
32	P0.6	I/O	Bit6 of Port 0
	CH4	I	Analog Input Ch4
	CAP1	I	Capture Input 1
33	P0.5	I/O	Bit5 of Port 0
	CH3	I	Analog Input Ch3
	IR1	I	IR receiver signal input 1
34	P0.4	I/O	Bit4 of Port 0.
	CH2	I	Analog Input Ch2.
35	P0.3	I/O	Bit3 of Port 0.
	OP1N	0	OP1-Amp N- Input
36	P0.2	I/O	Bit2 of Port 0.
	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	I	OP1-Amp P-Input.
37	P0.1	I/O	Bit1 of Port 0.
	OP0N	I	OP0-Amp N-Input.
38	P0.0	I/O	Bit0 of Port 0.
	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP0-Amp P- Input.
39	OP_VOUT	O	OPA output
40	OP_VINN	I	OPA N-Input
41	OP_VINP	I	OPA P-Input
42	P1.6	I/O	Bit6 of Port 1.
	AOCP	I	Analog OCP Control.
43	P1.7	I/O	Bit7 of Port 1.
	DOCPN	I	Digital OCP Control.
44	VCC_LDO	Power	LDO 5V power supply.
45	LDO_5	Power	5V output of LDO.
46	PGND	Ground	Power ground.
47	NC		
48	VCC_8	O	LDO VCC_8 output