CGF002A
Data Sheet

8Bit Single-Chip Microcontroller

Version: V0.0

Features

Motor Driving Engine (MDE)

- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC) Sine-Wave Solutions
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Position Detection (IPD)
- Programmable Dead-Time
- Independent PI Controller
- Independent General Low Pass Filter
- Frequency Generator

Embedded MCU

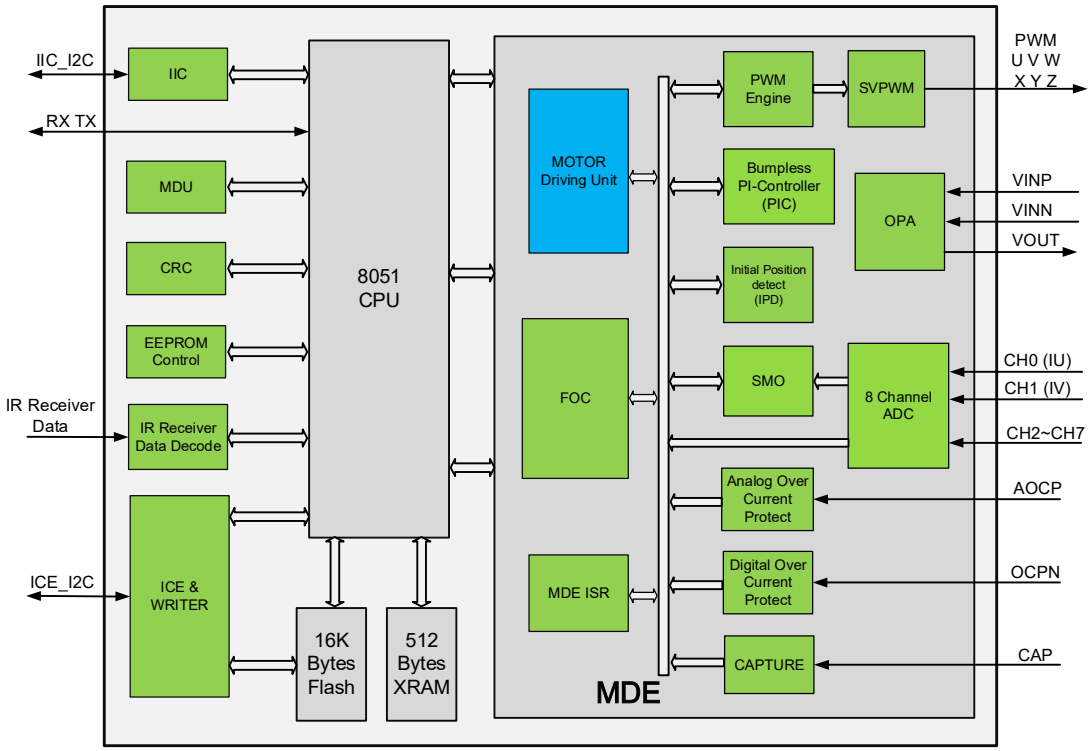
- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
- 2 External Interrupts (INT0N, INT1N)
- 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 16KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- 256 Byte EEPROM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
  8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- IIC Interface (Master/Slave Mode)
- One Wire RF/IR Receiver Output Signal Decode
- CRC16-CCITT Function
- Independent General PWM
- External Capture
- Internal Capture
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bitnormalization

List of Contents

1. General Description

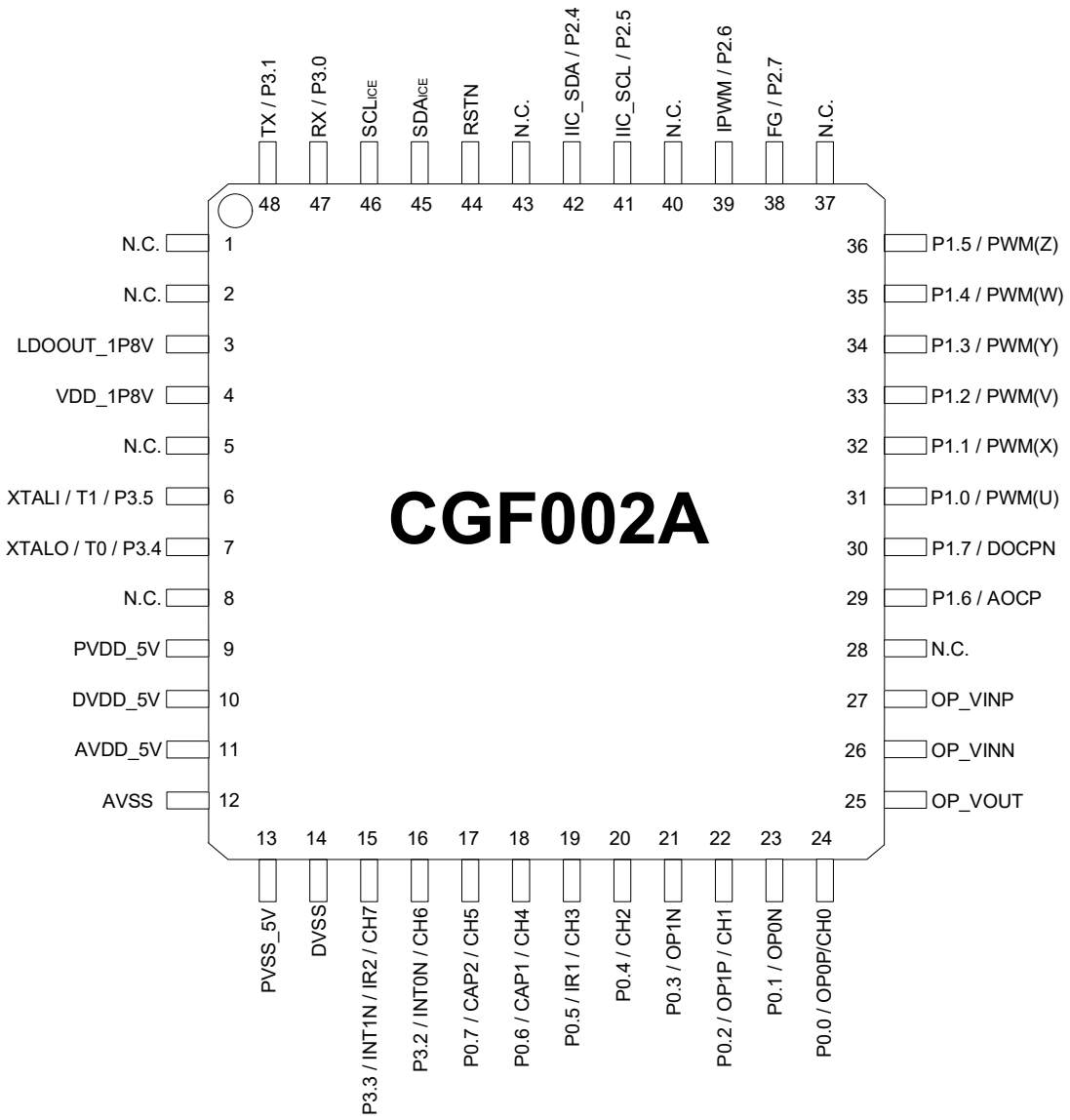
The CGF002A is a highly integrated motor drive controller. The CGF002A is composed of FOC sensor-less MCU for household fan、water pump、industry fan…etc.

2. Block Diagram



3. Pin Configurations

3.1. Package Instruction LQFP7x7- 48



3.2. Pin Description

Table 3.1. Pin Description

Pin #	Name	Type	Description
1	N.C.		
2	N.C.		
3	LDOOUT_1P8V	O	1.8V Voltage Output. **A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS**
4	VDD_1P8V	Power	1.8V voltage input for MCU and MOC block, can connect to LDOOUT_1P8V or external power source
5	N.C.		
6	P3.5	I/O	Bit 5 of Port 3
	XTALI	I	Crystal input pin. **Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS**
	T1	I	TIMER1 External Input
7	P3.4	I/O	Bit 4 of Port 3
	XTALO	O	Crystal output pin. **Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS**
	T0	I	TIMER0 External Input
8	N.C.		
9	PVDD_5V	Power	5.0V voltage input for I/O PAD. **A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS**
10	DVDD_5V	Power	5.0V voltage input for digital circuit in analog block. **A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS**
11	AVDD_5V	Power	5.0V voltage input for analog block. **A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS**
12	AVSS	Ground	Analog block power ground
13	PVSS_5V	Ground	I/O power ground
14	DVSS	Ground	Digital block power ground
15	P3.3	I/O	Bit 3 of Port 3
	CH7	I	Analog Input Ch7
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger
	IR2	I	IR receiver signal input 2
16	P3.2	I/O	Bit2 of Port 3
	CH6	I	Analog Input Ch6
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger
17	P0.7	I/O	Bit7 of Port 0
	CH5	I	Analog Input Ch5
	CAP2	I	Capture Input 2
18	P0.6	I/O	Bit6 of Port 0
	CH4	I	Analog Input Ch4
	CAP1	I	Capture Input 1
19	P0.5	I/O	Bit5 of Port 0
	CH3	I	Analog Input Ch3
	IR1	I	IR receiver signal input 1
20	P0.4	I/O	Bit4 of Port 0.
	CH2	I	Analog Input Ch2.
21	P0.3	I/O	Bit3 of Port 0.
	OP1N	0	OP1-Amp N- Input
22	P0.2	I/O	Bit2 of Port 0.

	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	I	OP1-Amp P-Input.
23	P0.1	I/O	Bit1 of Port 0.
	OP0N	I	OP0-Amp N-Input.
24	P0.0	I/O	Bit0 of Port 0.
	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP0-Amp P- Input.
25	OP_VOUT	O	OPA output
26	OP_VINN	I	OPA N-Input
27	OP_VINP	I	OPA P-Input
28	N.C.		
29	P1.6	I/O	Bit6 of Port 1.
	AOCP	I	Analog OCP Control.
30	P1.7	I/O	Bit7 of Port 1.
	DOCPN	I	Digital OCP Control.
31	P1.0	I/O	Bit0 of Port 1.
	PWM_U	O	PWM output. High-side PWM of phase U.
32	P1.1	I/O	Bit1 of Port 1.
	PWM_X	O	PWM output. Low-side PWM of phase X.
33	P1.2	I/O	Bit2 of Port 1.
	PWM_V	O	PWM output. High-side PWM of phase V.
24	P1.3	I/O	Bit3 of Port 1.
	PWM_Y	O	PWM output. Low-side PWM of phase Y.
35	P1.4	I/O	Bit4 of Port 1.
	PWM_W	O	PWM output. High-side PWM of phase W.
36	P1.5	I/O	Bit5 of Port 1.
	PWM_Z	O	PWM output. Low-side PWM of phase Z.
37	N.C.		
38	P2.7	I/O	Bit7 of Port 2.
	FG	O	Function Generate Output
39	P2.6	I/O	Bit6 of Port 2.
	IPWM	O	Independent User PWM Output
40	N.C.		
41	P2.5	I/O	Bit5 of Port 2.
	IIC_SCL	O	IIC clock
42	P2.4	I/O	Bit4 of Port 2.
	IIC_SDA	O	IIC data
43	N.C.		
44	RSTN	I	System Reset.

45	SDA_{ICE}		For ICE.
46	SCL_{ICE}		For ICE.
47	P3.0	I/O	Bit0 of Port 3.
	RX	I	Serial Data Transmit (UART)
48	P3.1	I/O	Bit1 of Port 3.
	TX	O	Serial Data Receive (UART)