

8051-Based MCU



CGF002A

Data Sheet

8Bit Single-Chip Microcontroller

Version: V0.0

Features

Motor Driving Engine (MDE)

- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC) Sine-Wave Solutions
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Position Detection (IPD)
- Programmable Dead-Time
- Independent PI Controller
- Independent General Low Pass Filter
- Frequency Generator

Embedded MCU

- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
- 2 External Interrupts (INT0N, INT1N)
- 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 16KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- 256 Byte EEPROM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- 8CH 10-bit ADC & 1CH 10-bit DAC
- Full Duplex UART Serial Channel
- IIC Interface (Master/Slave Mode)
- One Wire RF/IR Receiver Output Signal Decode
- CRC16-CCITT Function
- Independent General PWM
- External Capture
- Internal Capture
- Fast Multiplication-Division Unit (MDU):
16*16, 32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

List of Contents

1. General Description	8
2. Block Diagram	9
3. Pin Configurations	10
3.1. Package Instruction LQFP7x7- 48.....	10
3.2. Pin Description	11
4. Absolute Maximum Ratings	14
5. D.C. Characteristics	15
6. A.C. Characteristics	16
7. OPA Characteristics	17
8. A/D Converter Characteristics	17
9. Special Function Registers (SFR)	19
10. CGF002A SFRs and Reset Value	21
11. External Special Function Registers (XSFR).....	23
12. CGF002A XSFRs and Reset Value	23
13. Memory.....	25
13.1. Program Memory	25
13.2. Data Memory	25
13.2.1 Data Memory (IRAM)(00H~FFH).....	25
13.2.2 Data Memory (XRAM)(F000H~F1FFH)	25
14. Instruction Set	26
15. MCU	31
15.1 8051 Engine.....	31
15.1.1 ACC (Accumulator)	31
15.1.2 B (B Register)	31
15.1.3 PSW (Program Status Word Register).....	32
15.1.4 SP (Stack Pointer)	33
15.1.5 DP0 (Data Pointer 0).....	33
15.1.6 DP1 (Data Pointer 1).....	34
15.1.7 AUX(Auxiliary Register)	35
15.1.8 RCON (Internal RAM Control Register)	35
15.2 GPIO.....	36
15.2.1 Port	37
15.2.2 PINCONG (Pin Configure Register).....	38
15.2.3 PINSET (Pin I/O Setting Register)	40
15.3 Clock Structure	43
15.4 Timer.....	44
15.4.1 PFCN (Peripheral Frequency Control Register)	45
15.4.2 TMOD (Timer 0/1 Mode Register).....	46
15.4.3 TCON (Timer 0/1Control Register)	47
15.4.4 T2CON (Timer2 Control Register)	47
15.4.5 Timer0 Mode 0.....	49
15.4.6 Timer0 Mode 1	49
15.4.7 Timer0 Mode 2.....	49
15.4.8 Timer0 Mode 3.....	49
15.4.9 Timer1 Mode 0.....	50

15.4.10 Timer1 Mode 1	50
15.4.11 Timer1 Mode 2	50
15.4.12 Timer2 Mode 0	50
15.4.13 Timer2 Mode 1	51
15.4.14 Timer2 Mode 2	51
15.4.15 Timer2 Mode 3	51
15.5 Watchdog Timer	52
15.5.1 WDTC (Watchdog Timer Control Register)	53
15.5.2 TAKEY (Time Access Key Register)	54
15.5.3 WDTK (Watchdog Timer Refresh Key)	54
15.6 Serial Port (UART)	55
15.6.1 SCON (Serial Port Control Register)	58
15.6.2 SBUF (Serial Port Data Buffer)	60
15.6.3 SREL (Serial Port Reload Register)	60
15.7 Power Management	60
15.7.1 STOP MODE	60
15.7.2 IDLE MODE	61
15.8 Reset	62
15.9 Interrupt Controller	63
15.9.1 IEN0 (Interrupt Enable Register 0)	65
15.9.2 IEN1 (Interrupt Enable Register 1)	66
15.9.3 IRCON1 (Interrupt Request Register 1)	67
15.9.4 IP (Interrupt Priority Register)	68
16. 10-bit Analog-to-Digital Converter (ADC)	69
16.1 ADCCONT (ADC Control Register)	70
16.2 ADCSTR (ADC Start Convert and Setting Register)	71
16.3 ADCDLY (ADC Sample Delay Register)	72
16.4 ADC Data Register	73
16.5 ADC1 and ADC2 Offset Value Register	74
17. EEPROM	75
17.1 EE_ADDR (EEPROM Read/Write Address Register)	76
17.2 EE_DATA (EEPROM Read/Write Data Register)	76
17.3 EE_CMD (EEPROM Command Register)	76
18. IIC Emulation	77
18.1 IICCTL (IIC Control Register)	77
18.2 IICS (IIC Status Register)	78
18.3 IICA1 (IIC Address1 Register)	79
18.4 IICA2 (IIC Address2 Register)	80
18.5 IICRWD (IIC Read Write Data Register)	80
18.6 IICEBT (IIC Enable Transaction Register)	81
19. Capture	82
19.1 External Capture	83
19.1.1 EXT_CAPCONT (External Capture Control Register)	83
19.1.2 EXT_CAPT (External Capture Total Count)	84
19.1.3 EXT_CAPH (External Capture High-Level Count)	84
19.2 Internal Capture	85
19.2.1 INT_CAPCONT (Internal Capture Control Register)	85

19.2.2 INT_CAPT (Internal Capture Total Count).....	86
19.2.3 INT_CAPH (Internal Capture High-Level Count).....	86
20. Multiplication and Division Unit (MDU).....	87
20.1 MD_MODE (MDU Control Mode).....	87
20.2 MD_CONT (MDU Control Register).....	88
20.2.1 MDEF.....	88
20.2.2 MDOV	89
20.3 MD0 – MD5 (Multiplication Division Register).....	89
20.4 MDU Operation Description	90
20.4.1 Loading the MDx registers	90
20.4.2 Executing calculation	90
20.4.3 Reading the result from the MDx registers.....	90
20.4.4 Shifting.....	91
20.4.5 Normalizing.....	91
21. Cyclic Redundant Check (CRC).....	92
21.1 CRC_CTRL (CRC Control Register).....	93
21.2 CRC_DIN (CRC Data Register).....	93
21.3 CRC_DOUT (CRC Output Remainder Data Register).....	93
21.4 CRC_STR_BANK (Start Bank Index Register for Bank CRC Computation)	94
21.5 CRC_END_BANK (End Bank Index Register for Bank CRC Computation).....	94
22. Independent General PWM.....	95
22.1 IPWM_CTRL (Independent General PWM Register).....	95
22.2 IPWM_CYC (Independent General PWM Cycle Register).....	95
22.3 IPWM_DUTY (Independent General PWM Duty Register)	96
23. One Wire RF/IR Signal Decode	97
23.1 IR_DEC_SET (IR Data Decoder Setting Register)	97
23.2 IR_DEC_CTRL (IR Data Decoder Control Register).....	100
23.4 IR_HEADER_Z2 (IR Data Header Zone2 Cycle Register).....	101
23.5 IR_STOP_Z (IR Data STOP Zone Cycle Register)	101
23.6 IR_DOUT0~IR_DOUT5 (IR Decode Output Register Byte0 ~ Byte5).....	102
24. Software Reset	103
24.1 SOFT_RST_KEY (Software Reset Key Register).....	103
24.2 SOFT_RST_EN (Software Reset Enable Register).....	103
25. Motor Driving Engine (MDE)	104
25.1 MDE Architecture	104
25.2 Coordinate Transformation Block.....	105
25.2.1 Coordinate Transformation Block Architecture.....	105
25.2.2 CLAEKE Transform	105
25.2.3 PARK Transform	106
25.2.4 Coordinate Transformation Block description and setting	106
25.3 Current Control Loop Block.....	108
25.3.1 Current Control Loop Block Architecture.....	108
25.3.2 Current Control Loop Block description and setting	108
25.4 Inverse Coordinate Transformation Block	110
25.4.1 Inverse Coordinate Transformation Block Architecture.....	110
25.4.2 Inverse PARK Transform	110
25.4.3 Inverse CLARKE Transform.....	111

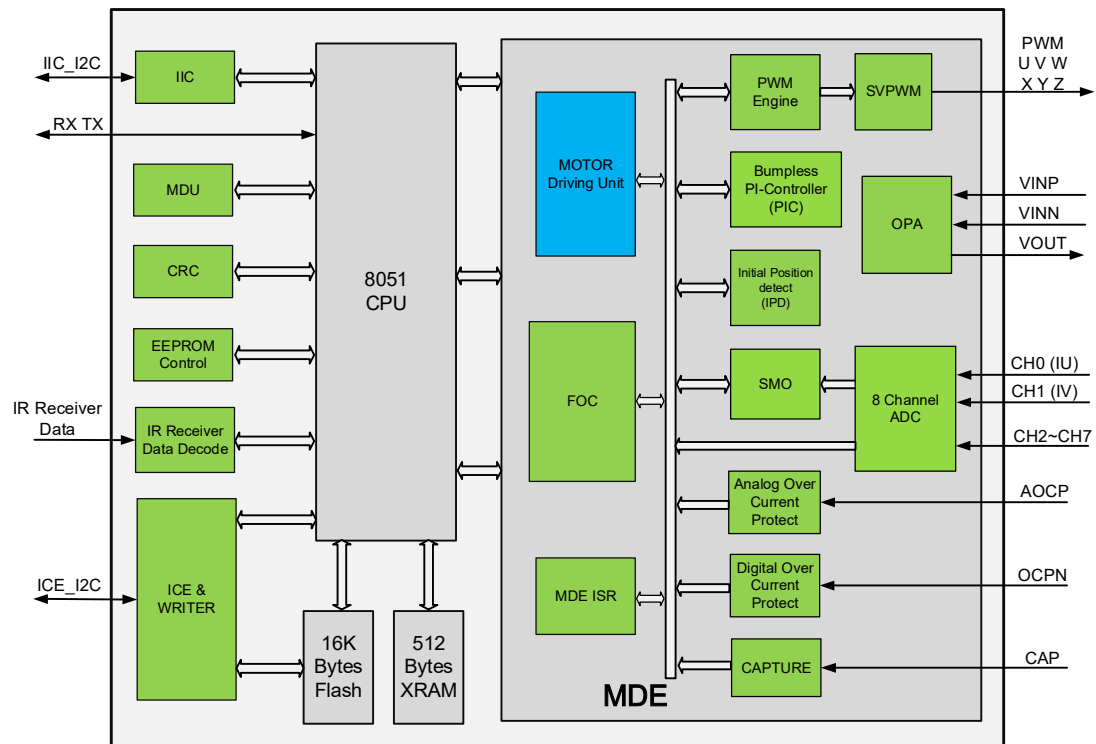
25.5 SMO Rotor Position Estimation Block	113
25.5.1 SMO Rotor Position Estimation Block Architecture	113
25.5.2 SENSORLESS FOC For PMSM	113
25.5.3 Motor Model	113
25.5.3 Current Observer	115
25.5.4 BEMF Estimation	116
25.5.5 Rotor Position Calculation	116
25.5.6 SMO Rotor Position Estimation Block description and setting	117
25.6 SVPWM Engine Block	118
25.6.1 SVPWM Engine Block Architecture	118
25.6.2 SVPWM Engine Block Architecture	118
25.6.3 7-Segment SVPWM	119
25.6.4 5-Segment SVPWM	120
25.6.5 SVPWM Over Modulation	120
25.6.6 Motor PWM Output Setting	121
25.7 Speed Control Loop Block	125
25.7.1 Speed Control Loop Block Architecture	125
25.7.2 Speed Control Loop Block description and setting	125
25.8 PI Controller	127
25.8.1 PI Controller Block Architecture	127
25.8.2 PI controller Block description and setting	127
25.8.3 User PI controller Block description and setting	130
25.9 IPD (Initial Position Detection)	131
25.9.1 IPD Control Register	131
25.9.2 IPD Pattern Define Register	132
25.10 OCP (Over Current Protection)	134
25.10.1 OCP Block Architecture	134
25.10.2 OCP Block description and setting	134
25.11 GEN_LPF (General Low-Pass Filter)	136
25.11.1 LPF Block Architecture	136
25.10.2 LPF Block description and setting	136
25.12 FG (Frequency Generator Control)	138
25.12.1 FG Control	138
25.13 MDE SFR List	139
25.13.1 MOTOR_CONT1 SFR	139
25.13.2 MOTOR_CONT2 SRF	139
25.13.3 Field Oriented Control SFR	141
25.13.4 PI_GAIN SFR (PI- Controller GAIN)	142
25.13.5 PI_TMSR SFR (PI Tracking Mode Select Register)	143
25.13.6 SP_CYC SFR	143
25.13.7 PI-Control Data SFR	144
25.13.8 Sliding Mode Observer Data SFR	146
25.13.9 Field Oriented Controller Data SFR	146
25.13.10 MPWMCONT SFR	147
25.13.11 MPWMDT SFR	148
25.13.12 MPWMINV SFR	148
25.13.13 MPWM DATA SFR	148

25.13.14 Analog OCP Control SFR	149
25.13.15 DOCPN Control SFR	150
25.13.16 IPD Control SFR	150
25.13.17 IPD Data SFR	151
25.13.18 General Low Pass Filter SFR.....	152
25.13.19 FG Control Register SFR.....	152
25.13.20 Coordinate Transformation Block Signals observe XSFR.....	153
25.13.21 Inverse Coordinate Transformation Block Signals observe XSFR	153
25.13.22 BEMF Estimation Signals observe XSFR	153
26. SYNC	154
27. Package Information	155
27.1 LQFP-48 7x7mm (AD48) Outline Dimensions	155
27.2 Marking Distinguish.....	156
27.2.1 Standard Ink (w/o code).....	156
27.2.2 Customization Ink (with customization code)	156
28. Ordering Information	157
28.1 Standard Product Name.....	157
28.2 Customization Product Name	157
29. Revision History	158
30. Disclaimers	159

1. General Description

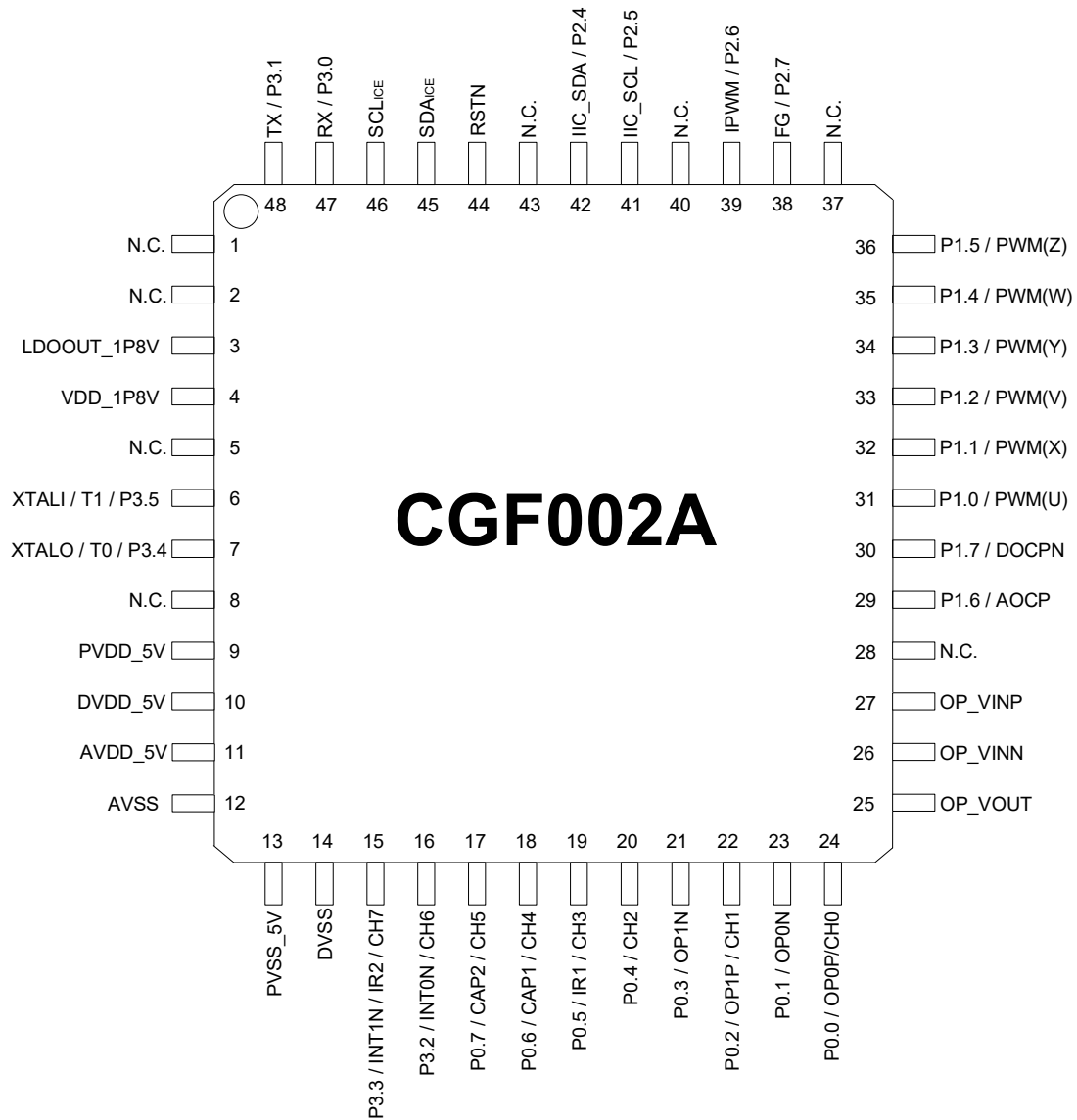
The CGF002A is a highly integrated motor drive controller. The CGF002A is composed of FOC sensor-less MCU for household fan、water pump、industry fan...etc.

2. Block Diagram



3. Pin Configurations

3.1. Package Instruction LQFP7x7- 48



3.2. Pin Description

Table 3.1. Pin Description

Pin #	Name	Type	Description
1	N.C.		
2	N.C.		
3	LDOOUT_1P8V	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS
4	VDD_1P8V	Power	1.8V voltage input for MCU and MOC block, can connect to LDOOUT_1P8V or external power source
5	N.C.		
6	P3.5	I/O	Bit 5 of Port 3
	XTALI	I	Crystal input pin. Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS
	T1	I	TIMER1 External Input
7	P3.4	I/O	Bit 4 of Port 3
	XTALO	O	Crystal output pin. Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS
	T0	I	TIMER0 External Input
8	N.C.		
9	PVDD_5V	Power	5.0V voltage input for I/O PAD. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS
10	DVDD_5V	Power	5.0V voltage input for digital circuit in analog block. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS
11	AVDD_5V	Power	5.0V voltage input for analog block. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS
12	AVSS	Ground	Analog block power ground
13	PVSS_5V	Ground	I/O power ground
14	DVSS	Ground	Digital block power ground
15	P3.3	I/O	Bit 3 of Port 3
	CH7	I	Analog Input Ch7
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger
	IR2	I	IR receiver signal input 2
16	P3.2	I/O	Bit2 of Port 3
	CH6	I	Analog Input Ch6
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger
17	P0.7	I/O	Bit7 of Port 0
	CH5	I	Analog Input Ch5
	CAP2	I	Capture Input 2
18	P0.6	I/O	Bit6 of Port 0
	CH4	I	Analog Input Ch4
	CAP1	I	Capture Input 1
19	P0.5	I/O	Bit5 of Port 0
	CH3	I	Analog Input Ch3
	IR1	I	IR receiver signal input 1
20	P0.4	I/O	Bit4 of Port 0.
	CH2	I	Analog Input Ch2.
21	P0.3	I/O	Bit3 of Port 0.
	OP1N	O	OP1-Amp N- Input
22	P0.2	I/O	Bit2 of Port 0.

	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	I	OP1-Amp P-Input.
23	P0.1	I/O	Bit1 of Port 0.
	OP0N	I	OP0-Amp N-Input.
24	P0.0	I/O	Bit0 of Port 0.
	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP0-Amp P- Input.
25	OP_VOUT	O	OPA output
26	OP_VINN	I	OPA N-Input
27	OP_VINP	I	OPA P-Input
28	N.C.		
29	P1.6	I/O	Bit6 of Port 1.
	AOCP	I	Analog OCP Control.
30	P1.7	I/O	Bit7 of Port 1.
	DOCPN	I	Digital OCP Control.
31	P1.0	I/O	Bit0 of Port 1.
	PWM_U	O	PWM output. High-side PWM of phase U.
32	P1.1	I/O	Bit1 of Port 1.
	PWM_X	O	PWM output. Low-side PWM of phase X.
33	P1.2	I/O	Bit2 of Port 1.
	PWM_V	O	PWM output. High-side PWM of phase V.
24	P1.3	I/O	Bit3 of Port 1.
	PWM_Y	O	PWM output. Low-side PWM of phase Y.
35	P1.4	I/O	Bit4 of Port 1.
	PWM_W	O	PWM output. High-side PWM of phase W.
36	P1.5	I/O	Bit5 of Port 1.
	PWM_Z	O	PWM output. Low-side PWM of phase Z.
37	N.C.		
38	P2.7	I/O	Bit7 of Port 2.
	FG	O	Function Generate Output
39	P2.6	I/O	Bit6 of Port 2.
	IPWM	O	Independent User PWM Output
40	N.C.		
41	P2.5	I/O	Bit5 of Port 2.
	IIC_SCL	O	IIC clock
42	P2.4	I/O	Bit4 of Port 2.
	IIC_SDA	O	IIC data
43	N.C.		
44	RSTN	I	System Reset.

45	SDA _{ICE}		For ICE.
46	SCL _{ICE}		For ICE.
47	P3.0	I/O	Bit0 of Port 3.
	RX	I	Serial Data Transmit (UART)
48	P3.1	I/O	Bit1 of Port 3.
	TX	O	Serial Data Receive (UART)